Recent progress in the development of 3D deep n-well CMOS MAPS

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In a deep n-well (DNW) monolithic active pixel sensor (MAPS) a full in-pixel signal processing chain is integrated by exploiting the triple well option of a deep submicron CMOS process. This work concerns with the design and characterization of DNW MAPS fabricated in a vertical integration (3D) CMOS technology. 3D processes can be very effective in overcoming typical limitations of monolithic active pixel sensors. This paper discusses the main features of a new analog processor for DNW MAPS (ApselVI) in view of applications to the SVT Layer0 of the SuperB Factory. It also presents the first experimental results from the test of a DNW-MAPS prototype in the GlobalFoundries 130nm CMOS technology.

Digital tier

ApselVI

Analog tier

DNW MAPS in 3D CMOS technology

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Introduction

One of the main concerns in the design of the ApselVI Front-end electronics is related to the voltage drop on analog power and ground lines. The final version of the MAPS detector is going to include 256x192 elements (with a 50μm pitch), each with a relatively high power consumption (ΔP≈32μA). Power distribution performed by means of a single thick metal sheet resistance = 30mΩ/μm (typ), width = 20μm both for power (AVDD) and ground (AGND) lines, 20mV voltage drop (ΔV) across both AVDD and AGND is expected.

This voltage drop may cause position dependent, systematic changes in the front-end features of functioning:

• DC voltage at the shaper output
• Gain
• Peaking time

A transconductor in the feedback network of the shaper (RC-CR) has the purpose of reducing the effects of voltage drop on the channel-to-channel dispersion of the DC voltage at the shaper output (ΔV).

• By using a transconductor, it is possible to set Vd to a given (chip) value through a voltage reference placed at the periphery of the chip, which is not affected by voltage drop issues

• Changes in peaking time and gain are mainly related to variations

• in the transconductor current (Itranscon)
• in the shaper input branch current (Iin)

The voltage drop issue has been addressed by means of the following current compensation scheme:

Voltage drop is simulated as a symmetrical voltage variation in the analog power (AVDD) and ground (AGND) lines.

Shaper output waveform obtained with (right) and without (left) voltage drop compensation for different values of Vd:

Percentage variation of the peaking time with and without compensation for different values of Vd:

Vd=1.5V, AVDD=1.5V-

Digital tier

Shaper

Preamplifier

Threshold

Correction

Gain

Charge Sensitivity [meV/keV]

INL = 2.3%

Threshold dispersion [±100e- / 13e-]

Conclusions

A new DNW monolithic sensor (ApselVI) for the SVT Layer0 of the SuperB factory has been designed. This MAPS prototype will be fabricated in the second multiproject run of the 3D IC Consortium.

Characterization of a DNW MAPS for ILC applications in the GlobalFoundries process

SD41 (Spin-Off Digital Readout) chip represents the first generation of 3D MAPS with advanced readout architecture for high data rate

Prototype designed for vertexing applications to the International Linear Collider (ILC) facility

Shaperless version of MAPS front-end with a pixel pitch of 20μm

Analog and digital tiers not yet connected. It is possible to test only the analog tier

Analog tier

Digital tier

Characterization of the 130nm CMOS technology provided by GlobalFoundries used for the Tezzaron 3D process is being carried out through test on the prototypes submitted in the First multiproject run