Recent progress in the development of 3D deep n-well CMOS MAPS

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In a DNW MAPS a full in-pixel signal processing chain is integrated by exploiting the triple well option of a deep submicron CMOS process. Various solutions complying with different sensor layout and pixel pitch have been fabricated in a planar (2D) 130nm CMOS technology. This work will discuss the design and characterization of deep N-well (DNW) monolithic active pixel sensors (MAPS) fabricated in a vertical integration (3D) CMOS technology. 3D CMOS technology could be very effective in overcoming typical limitations of monolithic active pixel sensors. The final paper will discuss the features of the front-end electronics with the first experimental results from the test of 3D DNW MAPS.

Summary 500 words

CMOS monolithic active pixel sensors (MAPS) may satisfy the requirements for highly granular, low mass detectors set by the experiments at the future high luminosity colliding machines such as the International Linear Collider (ILC) and the Super-B Factory. One of the main issues with CMOS MAPS is the design of a readout architecture with the capability to manage a large amount of data coming from large area pixellated detectors. For this purpose, a few years ago, a different kind of MAPS sensor, suitable for inclusion in a sparse readout scheme, was proposed. In the same substrate, such device, called deep n-well (DNW) MAPS, integrates a relatively large collecting electrode in a buried n-type layer and a fully CMOS signal processing chain. Many prototype chips have been fabricated and tested during a five year development activity. Recently, vertical integration processes have been taken into account for the design of 3D DNW MAPS. 3D circuit manufacturing involves the independent fabrication of two or more planar circuits on different wafers, which are subsequently bonded together after precise alignment and thinning. Among the available techniques for 3D stacking, the one developed by Tezzaron Semiconductor was chosen for the first Multi Project Wafer (MPW) run by the 3DIC international collaboration. This process, which relies upon the vertical integration of standard 130nm CMOS layers, has been used for the design of the first 3D DNW MAPS. Planar wafers for 2D testing have been fabricated and the characterization activity on the front-end electronics is ongoing. 3D prototypes are expected soon. The 3DIC collaboration has already planned a second MPW run which will start after the evaluation of the structures fabricated in the first run. The relevant design activity is already in progress. We plan to submit two different processors for hybrid pixels (32x128 pixels) and monolithic sensors (128x100 pixels) in view of applications to the SVT Layer0 of the SuperB Factory. The final paper will give an update on the status of 3D DNW MAPS design and show the experimental results of the first 3D prototypes.

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