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ASPIC: LSST camera readout chip

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The ASPIC chip has been designed to readout the 3.2Gpixels of the LSST camera focal plane. The dynamic range is more than 16 bit and the noise has to be less than 7μV rms with a crosstalk better than 0.05%. The architecture, chosen by LSST, is based on a "Correlated Double Sampling"with a "Dual Slope Integrator" method.
Many modular tests benches have been developed to qualify this chip and perform its integration inside the CCD readout chain.

Summary 500 words

The LSST camera will have more than 3000 video-processing channels. The readout of this large focal plane requires a very compact readout chain. The standard technique for analog signal processing of CCDs is "Correlated Double Sampling", implemented here with "Dual Slope Integrator"method. We have designed and implemented an ASIC for LSST: the Analog Signal Processing asIC (ASPIC). The goal is to amplify the signal close to the output, in order to minimize signal to noise ratio, and to send differential outputs to the digitization. Others requirements are that each chip should process the output of half a CCD, that is 8 channels and should operate at 173 K.
A specific Back End board has been designed especially for lab test purposes. It manages clocks, digitizes analog differentials outputs of ASPIC and stores data into a memory. It contains 8 ADC (18 bits) which are the LSST official choice, 512 kwords memory and an USB interface. A FPGA manages all signals from/to all components on board and generate the timing sequence for ASPIC. Its firmware is written in Verilog and VHDL languages. Internals registers permit to define various tests parameters of the ASPIC. A Labview GUI allows to load or update these registers and to check the good operating.
Several series of tests have been performed over the past year to characterize the ASPIC, at room or cold temperature (in particular linearity, noise and crosstalk). We have ramped up our acquisition and analysis capabilities.
Now, we work on the integration of the ASPIC and Back-End board with a CCD to measure the performance of the whole readout chain.

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