Conceptual design of a MGy tolerant integrated signal conditioning circuit in 130nm CMOS

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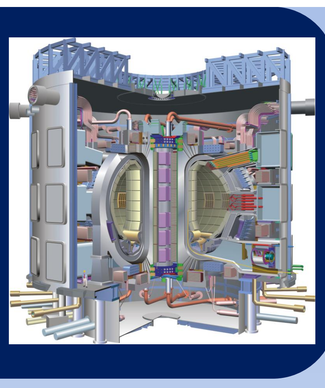
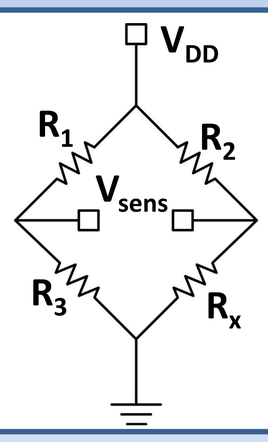
Abstract - The conceptual design of a MGy tolerant configurable discrete time signal conditioning circuit in a 0.13 and 0.7µm CMOS technology is presented, for use with resistive sensors like strain gauge pressure sensors. The design features a differential preamplifier using a Correlated Double Sampling (CDS) architecture at a sample rate of 20kHz. Furthermore, a high voltage buffer and level shifter is presented in the 0.7µm design. The gain is digitally controllable between 27 and 400. The nominal input referred noise voltage is only 8.6µV at room temperature. The circuits have a simulated radiation tolerance of more than 1MGy. Simulations were based on results obtained from [1,2].



Architectures and simulations

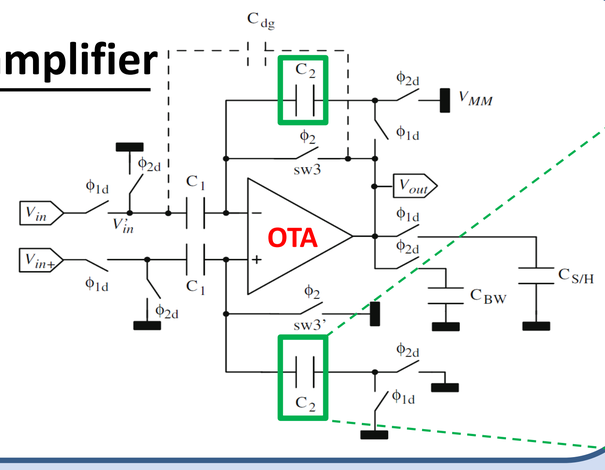
Input

millivolt signal form Wheatstone bridge



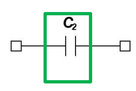
Architecture preamplifier

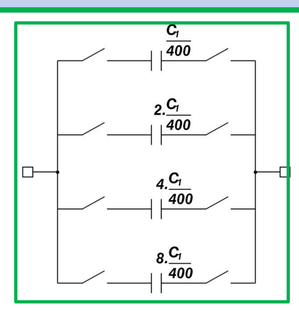
The circuit uses an folded cascode OTA in switched capacitor correlated double sampling configuration [3].



Gain control

$$A_v = \frac{C_1}{C_2}$$





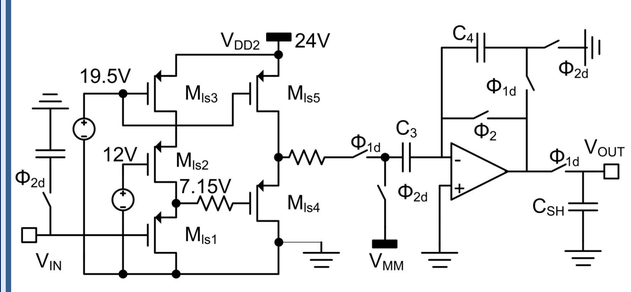
$$A_v = \left.\frac{400}{n}\right|_{n=1:15}$$

Design 0.7um

Maximum Vth shifts [1]

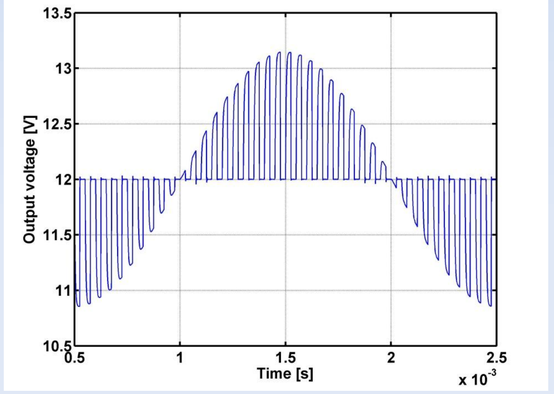
TID (MGy)	1
Vth_{NMOS}	-500mV
Vth_{PMOS}	+500mV

Voltage buffer and level shifter



- Integration of high voltage buffer
- High output swing
- Input noise = 8.5µV or 22nV/√(Hz)
- P_{PREAMP} = 1mW

Output of complete amplifier for 500Hz and 1mV input.

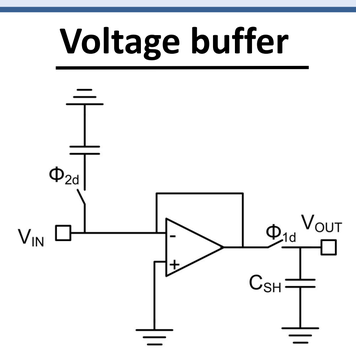


Design 0.13um

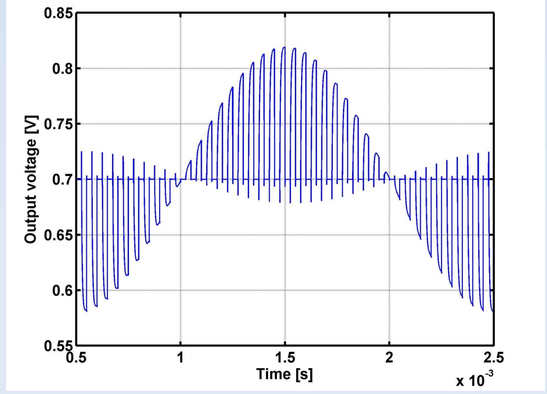
Maximum Vth shifts [2]

TID (MGy)	1
Vth_{NMOS}	-40mV
Vth_{PMOS}	+45mV

Voltage buffer

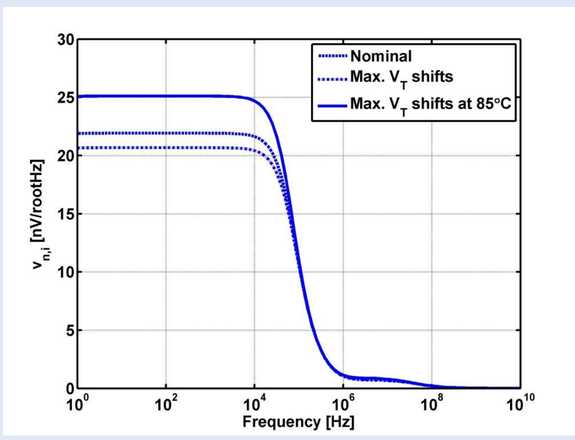


Output of complete amplifier for a 500Hz and 300µV input

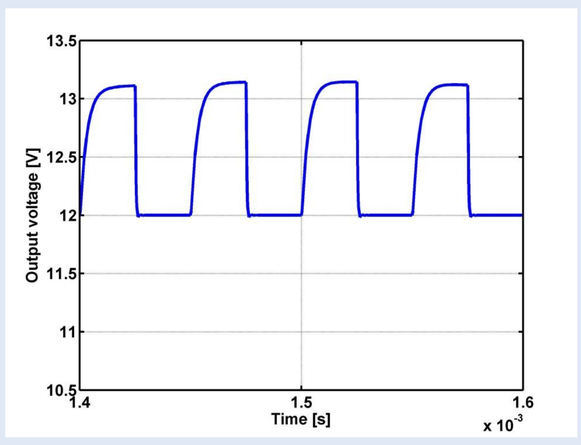


- Lower output swing
- Input noise = 8.6µV or 22nV/√(Hz)
- P_{PREAMP} = 1.5mW

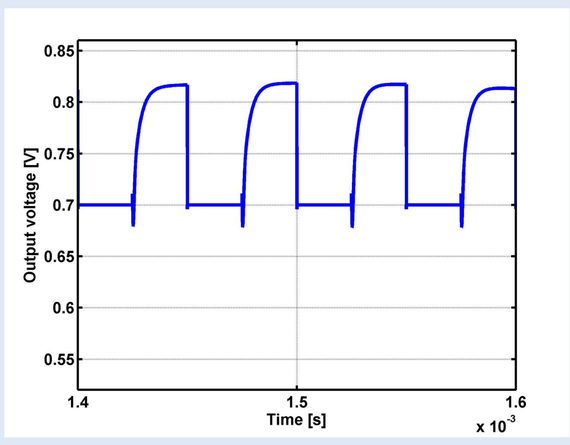
Temperature and Radiation behavior



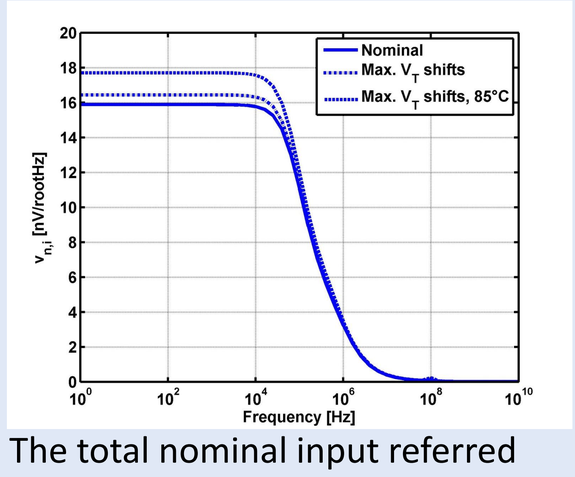
The total nominal input referred integrated noise voltage is 8.5 µV , 8.3µV after irradiation and 9.2 µV after irradiation at 85°C



OTA output voltage for a 3mV 500Hz input and a gain setting of 400. Remains identical after 1MGy.



OTA output voltage for a 300µV 500Hz input and a gain setting of 400. Remains identical after 1MGy.



The total nominal input referred integrated noise voltage is 8.6 µV , 9µV after irradiation and 9.6 µV after irradiation at 85°C

Conclusion – The conceptual design of a instrumentation amplifier has been presented showing a 1MGy radiation tolerance within a temperature ranging from 0°C to 85°C. The CDS architecture offers the benefit of intrinsic rejection of both offset and 1/f noise. This is especially important in radiation environments as the 1/f noise, related to surface defects, tends to increase under radiation as defects are created at the gate oxide channel interface. Furthermore, both designs show that the voltage gain has a guaranteed accuracy of 1.5% over the whole gain range under extreme conditions. In addition, the 0.7 µm design presents a buffer which allows high voltage output levels.

References:

[1] P. Leroux, S. Lens, M. Van Uffelen, W. De Cock, M. Steyaert, F. Berghmans, "Design and Assessment of a Circuit and Layout Level Radiation Hardened CMOS VCSEL Driver", IEEE TNS, vol. 54, pp. 1055-1060, Aug. 2007.

[2] F. Faccio and G. Cervelli, "Radiation induced edge effects in deep submicron CMOS transistors", IEEE TNS, Vol.52, no.6, pp. 2413-2420, Dec. 2005

[3] W. Claes, W. Sansen and R. Puers, "Design of Wireless Autonomous Datalogger IC's", published by Springer, 2005.