Contribution ID: **30** Type: **Poster**

Conceptual design of a MGy tolerant integrated signal conditioning circuit in 130 nm CMOS

Thursday 29 September 2011 16:00 (2h 30m)

The design of a radiation tolerant configurable discrete time signal conditioning circuit in 130nm CMOS technology for use with resistive sensors like strain gauge pressure sensors is presented. The circuit is intended to be used for remote handling in harsh environments in the International Experimental Thermonuclear fusion Reactor (ITER). The design features a 1.5V differential preamplifier using a Correlated Double Sampling (CDS) architecture at a sample rate of 20kHz. The gain is digitally controllable between 27 and 400. The nominal input referred noise voltage is only 12μV at room temperature. The circuit has a simulated radiation tolerance of more than 1MGy.

Summary 500 words

The design of a radiation tolerant configurable discrete time signal conditioning circuit in 130 nm CMOS technology for use with resistive sensors like strain gauge pressure sensors is presented. The circuit is intended to be used for remote handling in harsh environments in the International Experimental Thermonuclear fusion Reactor (ITER). In addition, it could serve to various other applications requiring a guaranteed functionality in these extreme environments. Examples of these applications can be the LHC (Large Hadron Collider) at CERN or the MYRRHA (Multi-purpose Hybrid Research Reactor for High-tech Applications) reactor at the SCK in Mol. The design features a 1.5 V differential preamplifier using a Correlated Double Sampling (CDS) architecture at a sample rate of 20 kHz. The gain is digitally controllable between 27 and 400. The nominal input referred noise voltage is only 12μV at room temperature. The circuit has a simulated radiation tolerance of more than 1 MGy.

Exposure to ionizing radiation is known to cause unwanted effects in CMOS circuit by changing the device characteristics. Therefore, it is necessary to design the circuit to compensate for these effects in order to ensure correct operation under radiation. Simulations were based on [1].

The circuit, designed in mainstream 130 nm CMOS technology consists of a switched capacitor CDS amplifier. Compared to classic continuous time instrumentation amplifiers, the switched capacitor architecture offers the benefit of intrinsic rejection of both offset and 1/f noise. This is especially important in radiation environments as the 1/f noise, related to surface defects, tends to increase under radiation as defects are created at the gate oxide channel interface. Both offset and 1/f noise are sampled in this CDS architecture during the reset phase and subtracted from the output during the subsequent amplification phase. The switches are realized with CMOS transmission gates. Dimensions are chosen to minimize clock feedthrough under normal operation.

The circuit uses an Operational Transconductance Amplifier (OTA) in switched capacitor feedback. The OTA is implemented as a wide-swing folded cascode amplifier with additional positive gain boosting feedback in the output stage. The circuit works with a power supply of 1.5 V. The OTA has an open loop gain of over 100 dB and a gain bandwidth product of 500MHz. The switched capacitive feedback is configurable through the use of a bank of binary scaled capacitors from 2 pF to 16 pF which are selectable using a digital control word. The input capacitance is 800 pF yielding a gain between 400 (2 pF feedback) and 27 (30 pF feedback).

[1] F. Faccio and G. Cervelli, "Radiation induced edge effects in deep submicron CMOS transistors. IEEE TNS (Dec. 2005), Vol.52, no.6, pp. 2413-2420.

Author: Prof. LEROUX, Paul (K.U. Leuven)

Co-authors: Mr VERBEECK, Jens (K.U.Leuven); Mr VAN UFFELEN, Marco (Fusion for Energy); Prof. STEYAERT, Michiel (K.U. Leuven)

Presenters: Mr VERBEECK, Jens (K.U.Leuven); Prof. LEROUX, Paul (K.U. Leuven)

Session Classification: Posters

Track Classification: ASICs