Comparison of single event effect robustness of dual and triple well technologies at the 90nm node

L. Pierobon, S. Bonacini, F. Faccio, A. Marchioro
CERN, European Organization for Nuclear Research, Geneva, Switzerland

Introduction

A candidate 90nm CMOS technology for an accelerator readout and control ASICs for LHC upgrades was characterized for Single-Event Effects (SEE). Amongst the latter, Single Event Upset (SEU) and Single Event Latch-up (SEL) were the most prominent. The circuits’ nodes deriving from scaling down both Vdd and the load capacitance. It is important to evaluate the SEE response in order to specify design rules or, in some cases, to evaluate the use of the circuit protection. This paper is focused on the study of the 90nm CMOS technology in terms of SEE. We study the impact of the use of a deep n+ to isolate the NMOS transistors from the substrate, and of the use of the multiple well (three devices in a p-well only directly in the n-well p-doped substrate). This has been long time considered a useful tool for reducing the SEE energies, but limits the depth of the charge collection compared to a single well implementation. This work is focused on obtaining a single bit error rate with the use of the deep n-well implant. We will refer to the latter configuration as Triple-Well (TW) and to the more conventional and as Dual-Well (DW).

Test structures

For this work, we chose to use the heavy ion irradiation facility of the Cyclotron Research Centre (CRC) at ICL, Louvain-la-Neuve, Belgium. The cross-section curve is plotted versus the LET. With such a curve, it is possible to estimate the error rate of different devices, and it can be used in virtually any radiation environment. Since the number of ions in the cocktail is limited to 4, it is customary to obtain additional points for the plot by ‘bitting’ the sample under test with respect to the ion beam. In this paper, we will report the results of ions with an LET increased by 1/10 (10%/100%/10% of the angle, where the angle is measured with respect to the normal (0%)).

The test was run static, holding the data in the registers for cycles of 3 seconds, plus a 1ms stream-in/stream-out for checking and refreshing data. The test pattern was a checkerboard (alternating ones and zeros). The measurement system allowed to record the position of each bit in error during the test, in turn enabling the reconstruction of Multiple Bit Upsets (MBU). In these events a number of physically adjacent bits are corrupted by the charge deposited by a single ion.

Clock tree design

The clock signals are provided from outside and are inverted at the clock root, then the resulting 4 clocks are distributed by separate trees of four levels of inverters each. In the design of the clock tree, optimization was done for the area occupation rather than for speed, and the resulting capacitive load at the output of Level 3 is estimated to about 70 fF, which includes the parasitic capacitance of the metal wiring (about 20 fF for the 200 um long metal lines).

SEUs in the latches

The cross-section curve for the sensitivity of each master-slave register to SEU is shown above for data taken at a voltage supply of 1.2 V. It is interesting to note how the trend is not monotonic, the cross-section decreasing at the LET of 21.3 MeVcm²/mg (this point refer to an irradiation at normal incidence, while the point at LET > 19.9 was taken at a grazing angle of 60 degrees). This trend is not useful for data sets taken at different angles of incidence in modern CMOS technologies. At larger angles the probability of MBUs increases because, due to the impression of density of bits in these technologies, neighbour registers collect fraction of the charge deposited by a single particle. As a consequence, it is rather at grazing angles often produces a larger number of errors – especially for high LET.

The following plots report the results of both DW and TW structures, for different energy levels, and for both single and multiple bit upset configuration.

Hits on the clock tree

Errors traceable to hits on the clock tree appear as an abnormally large number of bits in error in the same exposure period of 3 s; the analysis of the physical location of the erroneous bits reveals that they are driven by the clock buffer. Only certain glitches in the clock occurring at given hold states can induce the stored data to be corrupted. Since a checkerboard pattern is used for the test, a glitch in any clock buffer only induces errors (if any) in a bit of the output clock by a factor of 1/4.

The number of events traceable to hits in any level-3 buffer was limited to a total of 20 for the TW and 10 for the DW structures, for all these events the supply voltage and LET. None of these events was observed for an effective LET below 14.1 MeVcm²/mg, and the resulting cross-section for one event (where 32 bits are in error) normalizing the buffer was in the 5×10⁻¹⁰ cm² range, with small statistical significance. Even more rarely observed, the events traceable to hits in a level-2 buffer affect 320 bits out of 450 consecutive ones. Only 7 such events have happened during the full irradiation test for this level-2 buffer. For the highest effective LET of 24.6 MeVcm²/mg, for a resulting cross-section normalized to one buffer of about 6×10⁻¹² cm². One only event possibly related to a glitch in a level-1 buffer has been recorded, with 544 bits in errors mostly concentrated in one region and in alternate position, but with a large number of outliers (wrong bits in isolated random locations in the register). This happened also only for the largest effective LET used in the irradiation test.

Although all these errors due to glitches in the clock tree were observed for LETs equal or larger than those expected from recoils in an LHC-like radiation environment, this should not lead to the wrong general conclusion that they are not a concern. The occurrence of these events is heavily dependent on the specific implementation of the clock tree, and our results should rather be considered as a warning for the designers: clock trees should be carefully thought, implemented and simulated for particle charge ejection (hits) at the design stage.

Conclusions

The measured cross-section for the master-slave registers results to be comparable with available data in 130 nm CMOS processes. The systematic use of the available triple well option leads to a marginal decrease of the error rate in our application, but could still be considered interesting because it comes at no additional fabrication cost. The decrease of the supply voltage from the nominal 1.2 V down to 0.8 V only results in a total increase of 25% in area occupation, but it is very effective for the relevant resulting contribution in the power consumption. MBUs in registers are observed only at high LET, however, this conclusion might not apply to the much more aggressively packed pixels in SiPMs, for which a dedicated test should be run.

The sensitivity to Single Event Upset of latches designed in a 90nm dual and triple well CMOS technology has been measured irradiating a custom shift register with heavy ions. Latches designed with the NMOS transistors isolated from the substrate with a deep n+ (triple well) are only marginally less sensitive to SEUs, and only at high LET of the ions. The impact of lowering the voltage supply from 1.2 to 0.8V on the cross-section is limited to about 25%. Hits on the clock distribution network are observed and corrupt the data stored in multiple cells.