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Comparison of single event effect robustness of dual and triple well technologies at the 90 nm node

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As triple well technologies became available in recent years as an option for several submicron technologies, the question of their robustness against SEU with respect to single well versions has been asked, but a systematic comparison has been missing from the literature. This work present the first systematic comparison of the sensitivity to Single Event Upsets of latch cells designed in a 90nm CMOS and implemented in identical circuits realized in regular and isolated triple well technologies. Two types of CMOS latches were investigated: the first fabricated with NMOS transistors in a lightly doped p-well, while the second type, using identical layouts, was fabricated with isolated triple-well (deep buried n-well) NMOS transistors isolated from the p-substrate. The latter have shown a robustness increase to SEUs by a factor of 2 with respect to the former, albeit only at high LET of the ions. The impact on robustness of the voltage supply was also measured to be to about 20%. Finally, hits on the clock distribution network were observed corrupting the data stored in multiple cells.

Summary 500 words

In view of possible application in Front-End electronics design for the LHC upgrades, we have studied the Single Event Upset (SEU) sensitivity of latches designed in a commercial 90nm technology. The test vehicle for this investigation is a custom integrated circuit containing two shift registers, each composed of about 61k latches in master-slave configuration driven by two independent non-overlapping clocks with fully separated clock trees. The difference between the two cells resides in the technology choice: one uses NMOS transistors in the substrate, the other NMOS isolated via a buried n-well (triple well).

Irradiation with heavy ions of Linear Energy Transfer (LET) between 1.2 and 21.3 MeVcm-2mg-1, at different incident angles to the surface of the chip, has been performed at the cyclotron of CRC, Belgium. The chain of latches were exposed in data storage mode at different supply voltages: 1.2, 1 and 0.8V. An additional test with the latches constantly clocked at 5MHz has also been performed, evidencing little difference in sensitivity with respect to the data storage mode. Results are reported in terms of cross-sections, the ratio of the observed errors over the integral particle fluence during the test.

While single bit errors dominate the cross-section at low LETs, the contribution of double and even triple bit errors at high LET and incidence angle is significant. Latches in the isolated triple well turn out to be less sensitive, by a factor close to 2 at most, but only for LETs above 10 MeVcm-2mg-1. The influence of the supply voltage in the explored range is instead limited to cross-section variation of about 20% for all latches.

In addition to errors due to hits in the latches themselves, we observed a number of events attributable to hits in the clock tree of our test chip. Their signature –which has been shown to be compatible with the architecture of the clock tree circuit used - is the simultaneous corruption of half of the bits stored by all latches on the clock branch affected by the particle hit, with a maximum of 320 errors observed for a single strike. This effect is visible already for LETs below 14 MeVcm-2mg-1, a range accessible to fragments produced in Silicon in the LHC environment –although with relatively small probability. Despite their usually large capacitive loads, clock trees can be weak points in terms of sensitivity to single events and hence they will have to be carefully designed. No clock tree upset was observed at 10 MeVcm-2mg-1 and below.

Compared to available data for shift registers in a non-well isolated 130nm technology, the cross-sections in the two nodes are close to each other indicating similar sensitivity to SEUs.

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