Programmable Logic in the 21st Century

Where are we and Where are we going?

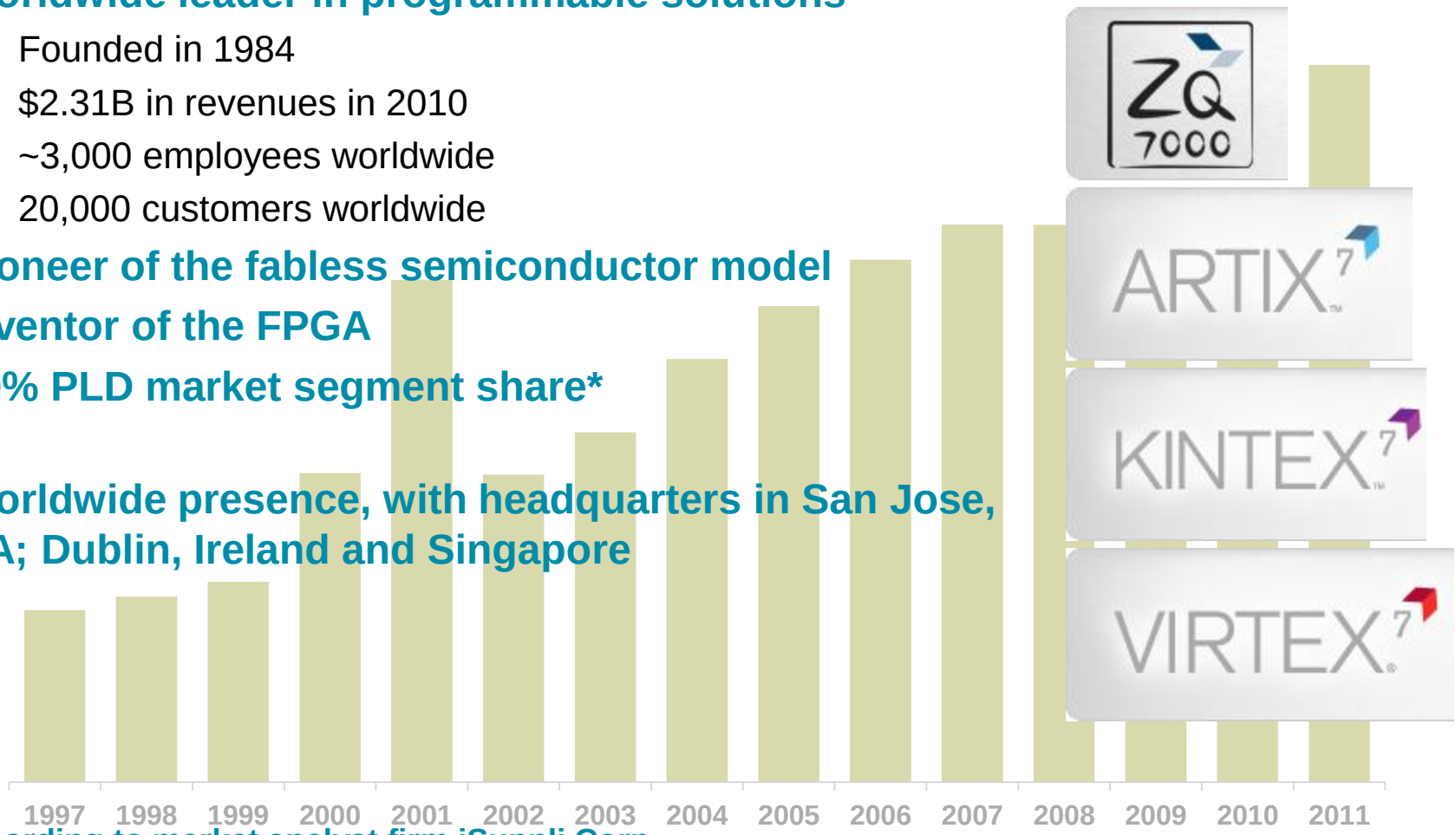
Steve Trimberger, Xilinx Fellow

Key Messages

- **Still Pushing IC Manufacturing Technology**
  - Programmable logic has been successful because of effective use of Moore's Law
  - Integrated circuit manufacturing doesn't give us all we need
  - More than Moore: 3D, circuits for power, rad-hard, integration
- **Xilinx 7-Series is Pretty Impressive**
  - Capacity, power, I/O bandwidth, processor integration, ADC
  - Xilinx targets its major markets: communications, computing, image processing, automotive, industrial control
- **Power: its Importance Continues to Grow**
  - FPGAs still give the best ops/watt
- **Design Effort**
  - Improved devices, architecture and software

Introducing Xilinx

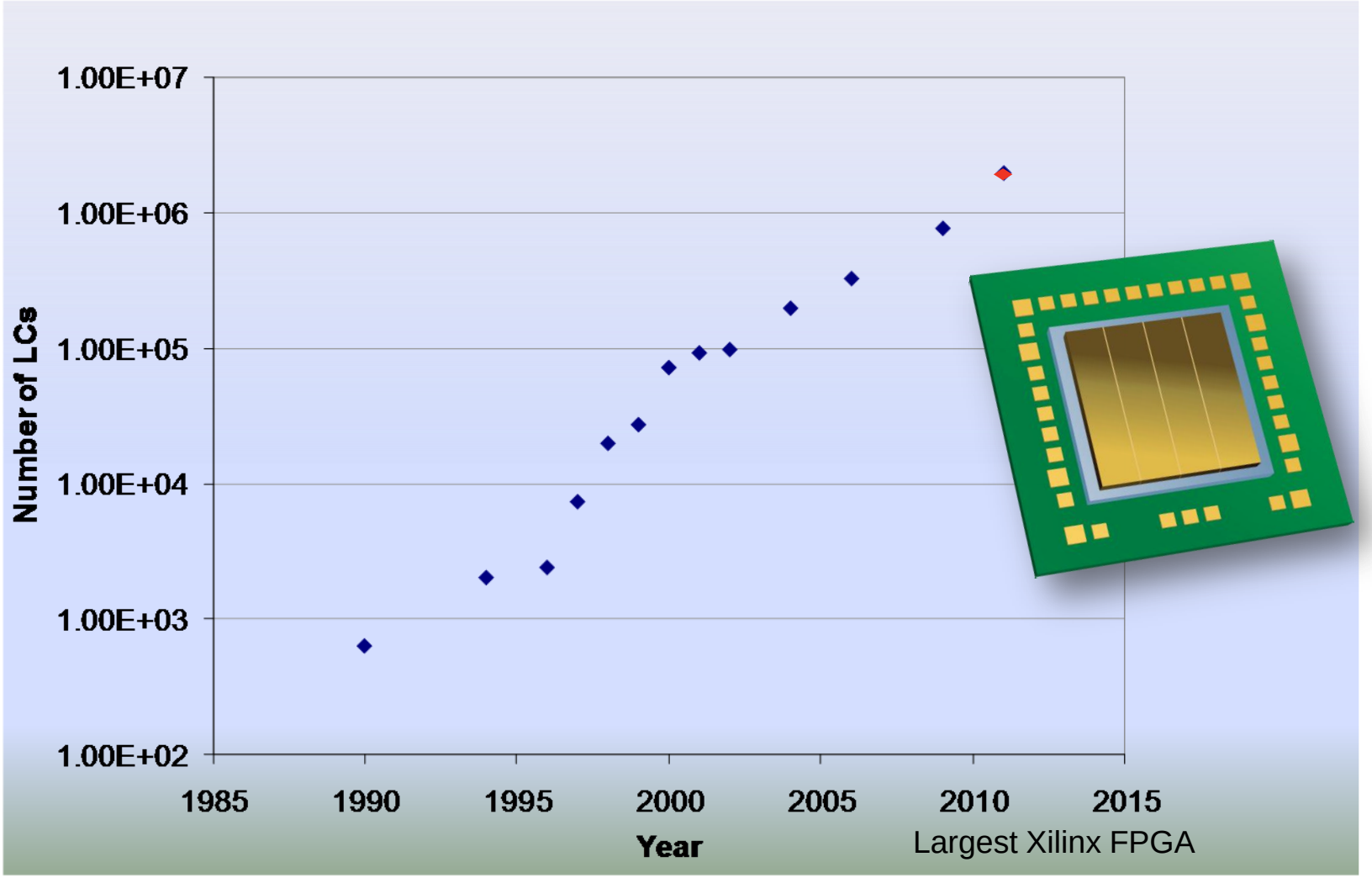
- **Worldwide leader in programmable solutions**
  - Founded in 1984
  - $2.31B in revenues in 2010
  - ~3,000 employees worldwide
  - 20,000 customers worldwide
- **Pioneer of the fabless semiconductor model**
- **Inventor of the FPGA**
- **50% PLD market segment share***
- **Worldwide presence, with headquarters in San Jose, CA; Dublin, Ireland and Singapore**



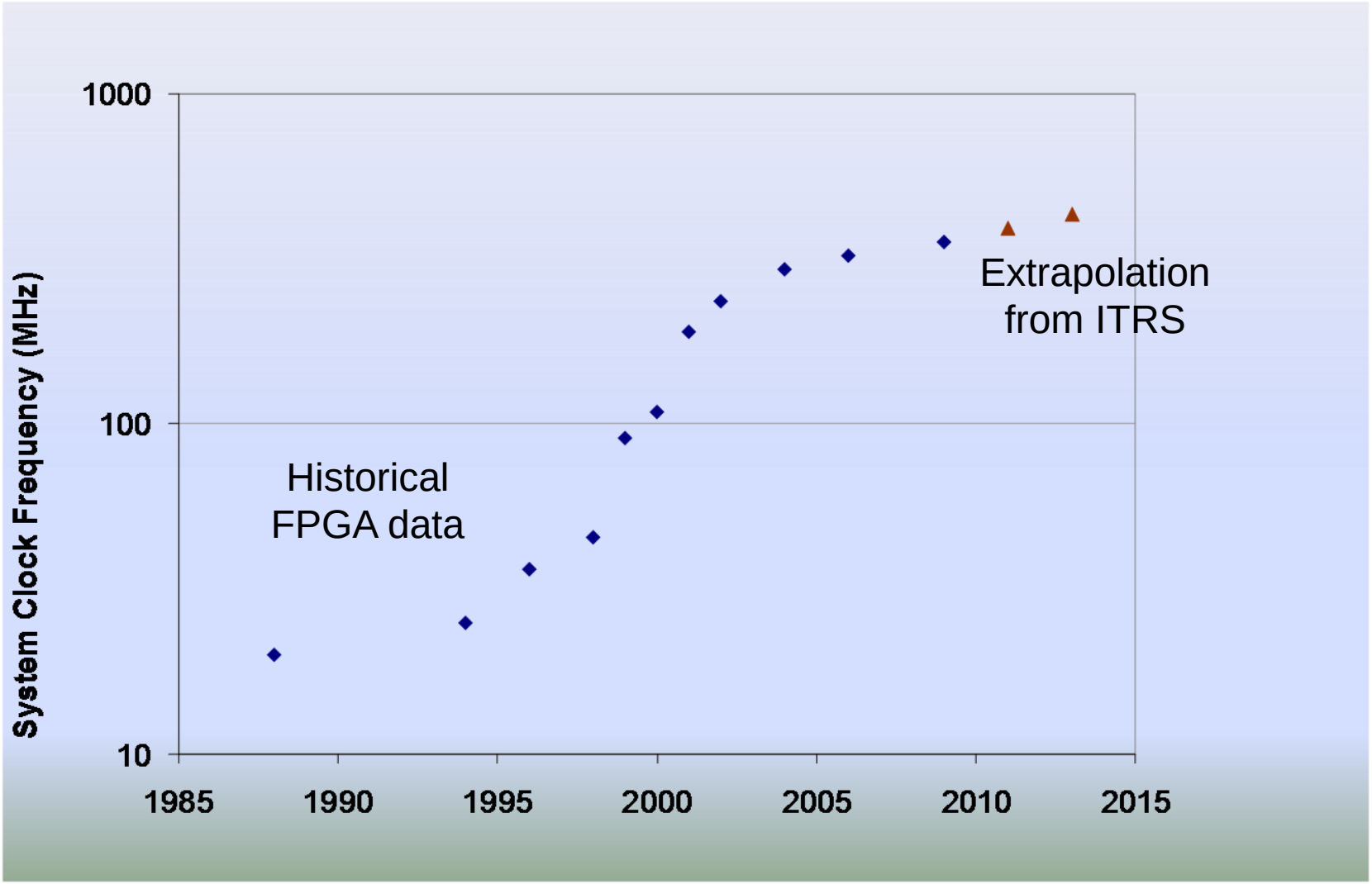
*** According to market analyst firm iSuppli Corp .**

Source: http://www.xilinx.com/company/about.htm

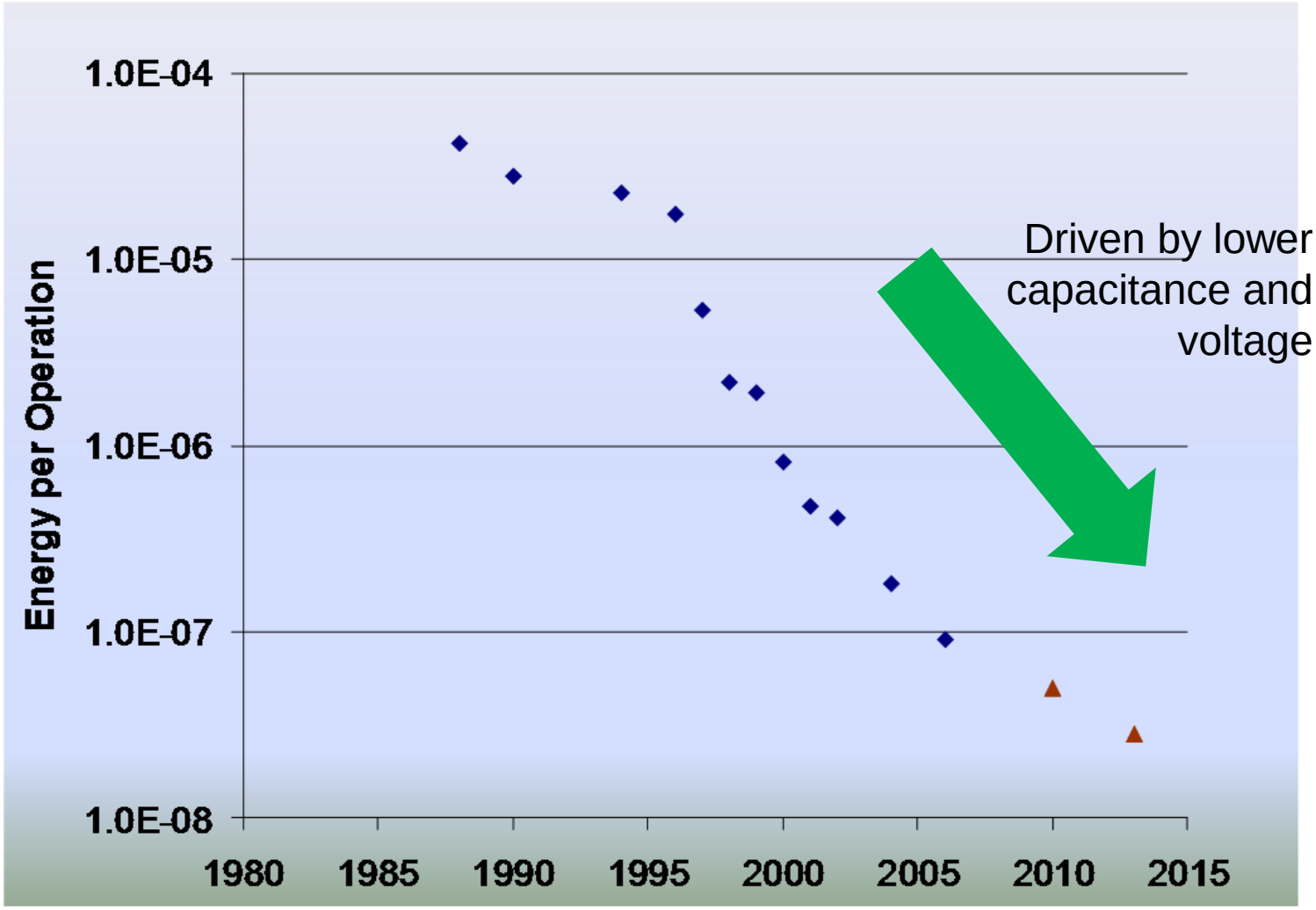
FPGA Capacity Trends



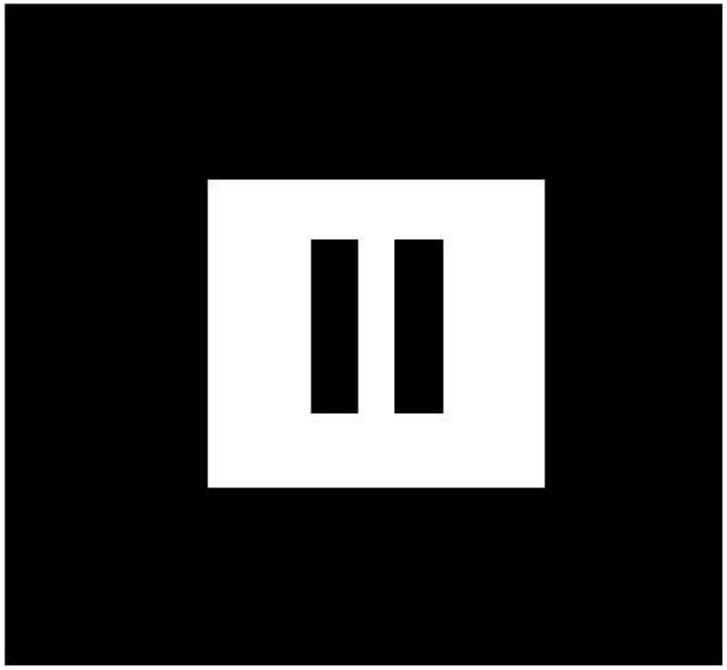
FPGA Performance Trends



FPGA Energy Trends (W / LC MHz)



Pause



Solving Next Generation Design Challenges For All Market Segments

Next Gen Wired Communications

Next Gen Wireless Communications

High Performance Computing

Consumer

ARTIX 7	KINTEX 7	VIRTEX 7
Lowest Power and Cost	**Industry's Best Price-Performance**	**Industry's Highest System Performance and Capacity**
• Portable/handheld ultrasound • 3D cameras & camcorders • D-SLR still cameras • Software defined radio • 3DTV • Portable eReaders • Automotive Infotainment • Multifunction printers	• Wireless LTE infrastructure • 10G PON OLT line card • LED backlit & 3D video displays • Video-over-IP bridge • Cellular radio • Medical & Avionics imaging • Set top boxes • Motor control	• 400G & 100G line cards • 300G Interlaken bridge • Terabit switch fabric • 100G OTN • MUXPONDER • RADAR • ASIC emulation • Test & Measurement

Aerospace & Defense

Test & Measurement

Medical Imaging

Audio Video Broadcast

Major Universal Market Challenges

Market Challenges

- **Lower Power**
  - Meeting Legislation and Regulations
- **Higher Performance**
  - System Capacity and Capability
- **Improved Productivity**
  - Reduce Capital and Operating Expenses (OPEX, CAPEX)

Market Segments Affected

Flat Panel/TV, Central Office, Server Farms, Portable Medica Portable and Wired Consumer

Wired Infrastructure, 400G Networks, Wireless, Broadcast, Defense

Wireless, Wired, High Performance Computing

#1 problem from over 300 top customers' surveyed:
Higher System Performance Impacted by Power Budget Limitations

Xilinx 7 Series Highlights

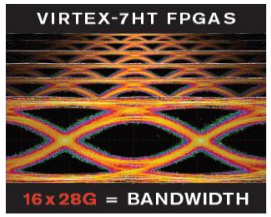
- **7 Series silicon devices**
  - **28 nm Technology, TSMC HPL process**
  - 50% reduction in power over 40 nm devices
- **3 FPGA Fabrics**
  - Artix = Low cost, low power FPGA (“1W FPGA”)
  - Kintex = Density & performance FPGA (“Market Sweet spot”)
  - Virtex = Highest density and performance FPGA (“More than Moore”)
- **‘More than Moore’ density increase**
  - Up to 2M logic cells
  - Using Stacked Silicon Interconnect Technology (SSIT)
- **Improved GT bandwidth**
  - **GT bandwidth increased to 28 GHz**
- **Zynq Embedded Processing Platform (EPP)**

Design Green **by Xilinx**

ARTIX 7

KINTEX 7

VIRTEX 7



ZYNQ

Ground Breaking Capacity Gains at 28nm

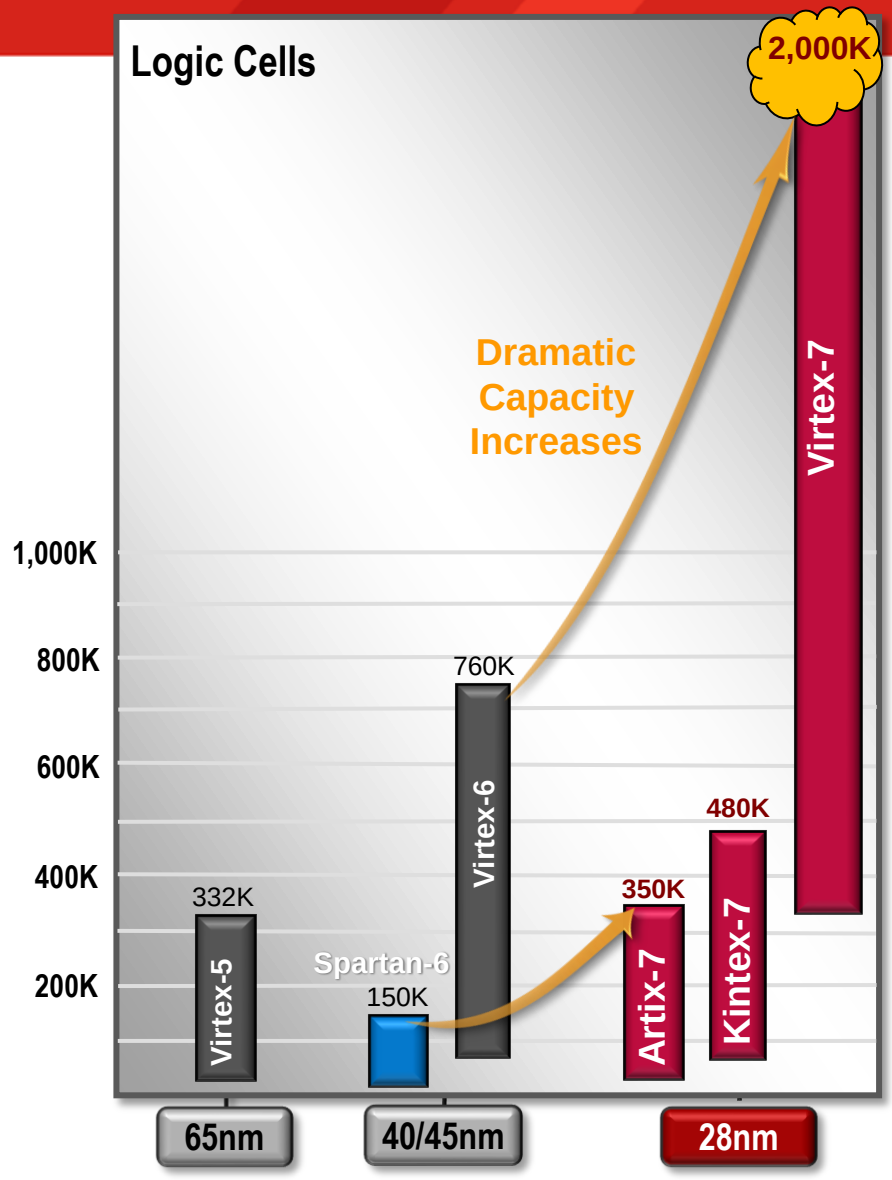
World's First 2 Million Logic Cell FPGA

- **Over 2x capacity increases over Spartan-6 and Virtex-6 FPGAs**

Family	Capacity Range
ARTIX-7	8K – **350K LCs**
KINTEX-7	70K – **480K LCs**
VIRTEX-7	330K – **2M LCs**

- **8K – 2M LCs; the widest capacity range offered in a single unified product family**

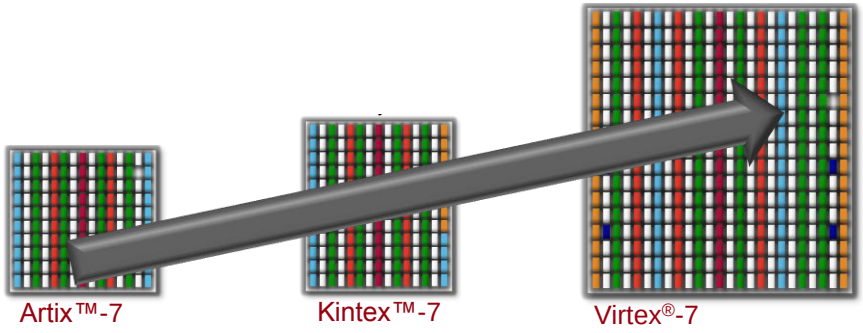
- **Larger densities enable higher performance**
  - More calculations/clock cycle by utilizing parallelism inherent in FPGAs



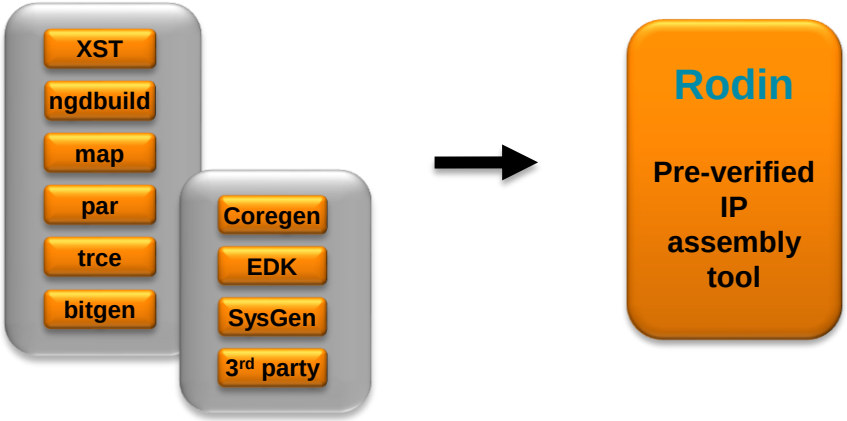
Unified Architecture Boosts Design Productivity

Accelerating Design Creation, Debug and Simplifying Reuse

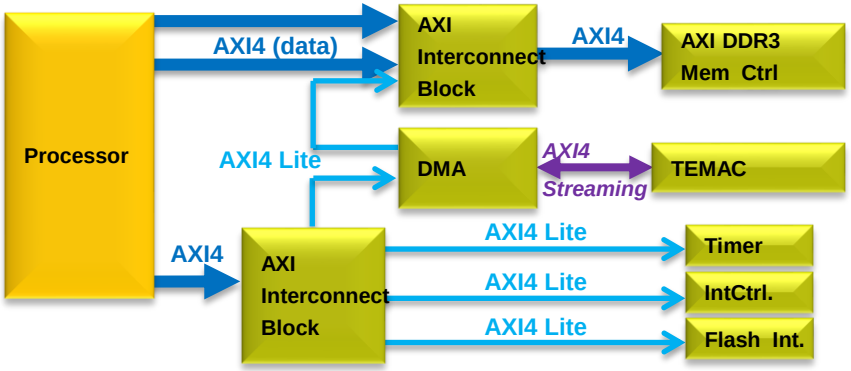
Unified HW Architecture



Unified SW Architecture

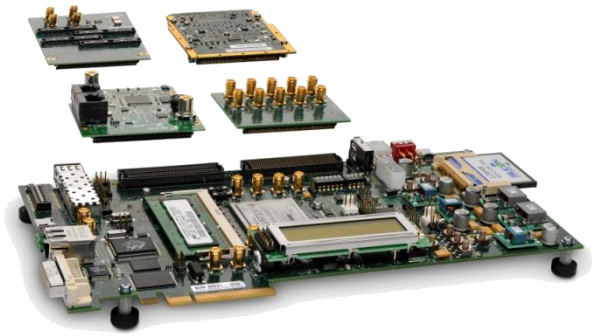


Plug & Play IP



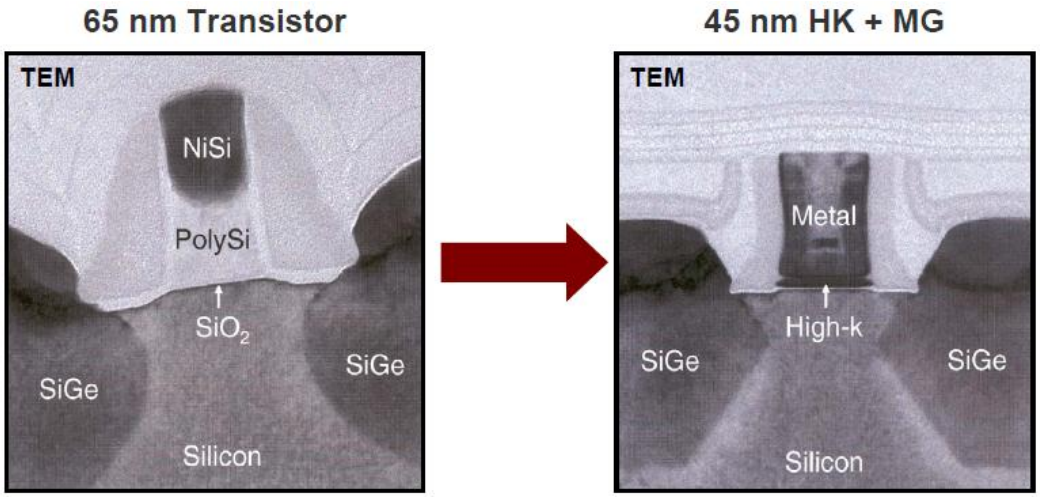
AMBA System Architecture IP-XACT IEEE P1735

Plug & Play Boards



High-k Metal Gate Transistor Rescues Moore's Law

The Transistor Re-Invented



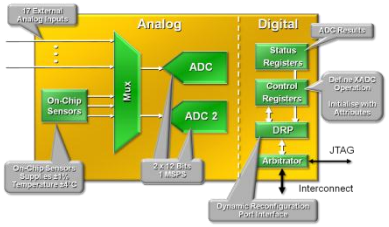
HKMG:
- introduced by Intel at 45nm
- available at 28nm from top foundries

> 25x lower gate oxide leakage
> 30% lower switching power
> 30% higher drive current or
> 5x lower source-drain leakage

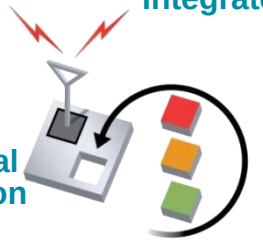
Source: "Challenges and Innovations in Nano-CMOS Transistor Scaling", Tahir Ghani, Intel , Oct 2009

7 Series Power Efficiency Focus from Every Angle

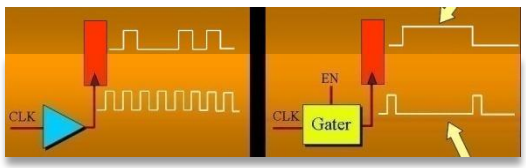
Additional Power Saving Features



Integrated Analog Front End



5th gen. partial reconfiguration



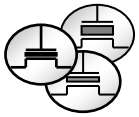
Fine grain clock and logic gating

Design Green

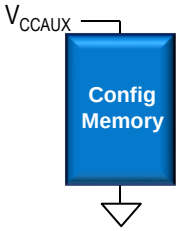
With Xilinx

Reducing Static Power

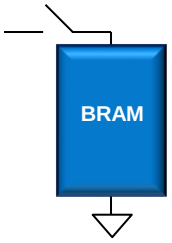
High performance, low power process



Transistor choice optimization



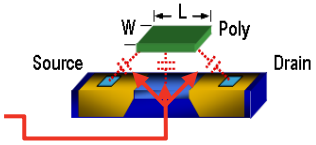
Reduced from 2.5V to 1.8V



Unused BRAM Power Savings

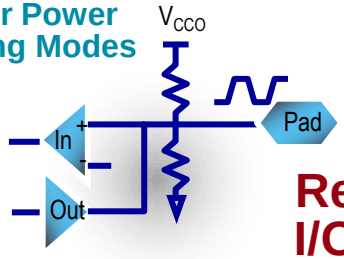
Reducing Dynamic Power

Process Shrink



Optimized Hard Blocks

IO Design & User Power Saving Modes



Reducing I/O Power

Lower device core voltage

-2L Xilinx 7 Series FPGAs

Xilinx History of Systems Integration

1986

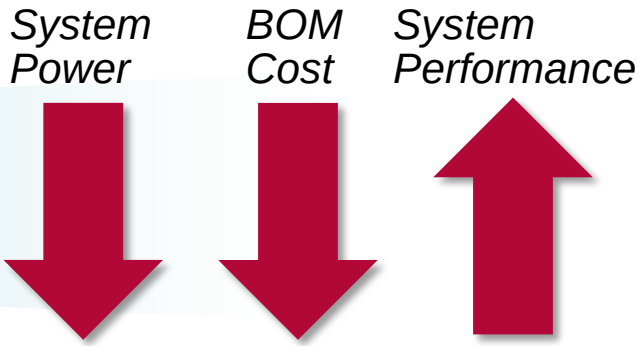
Oscillator
Distributed RAM
Block RAM
Dual Port RAM
CMOS / TTL Programmable I/O

2000

I/O Buffers with Programmable Drive Strength
Multi-Standard Programmable I/O Support
Phase Locked Loops
I/O Termination Impedance
DSP
LVDS Transceivers
Processor
Multi-Gigabit SerDes
Phase Multi-Mode Clock Generators
Mixed Signal System Monitor
PCI Interface
Ethernet MAC

2011

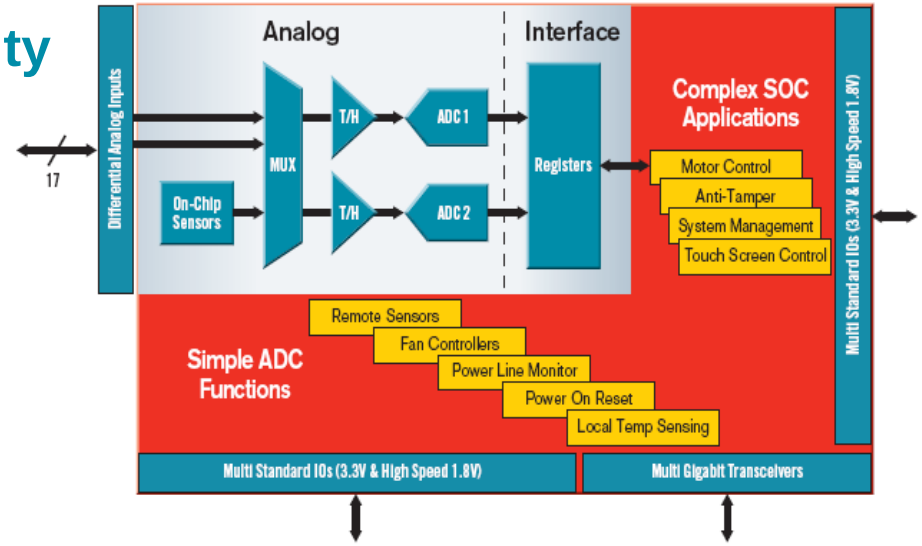
Stacked Silicon Interconnect
Agile Mixed Signal Converter
Extensible Processing Sub-system



Agile Mixed Signal (AMS) Technology

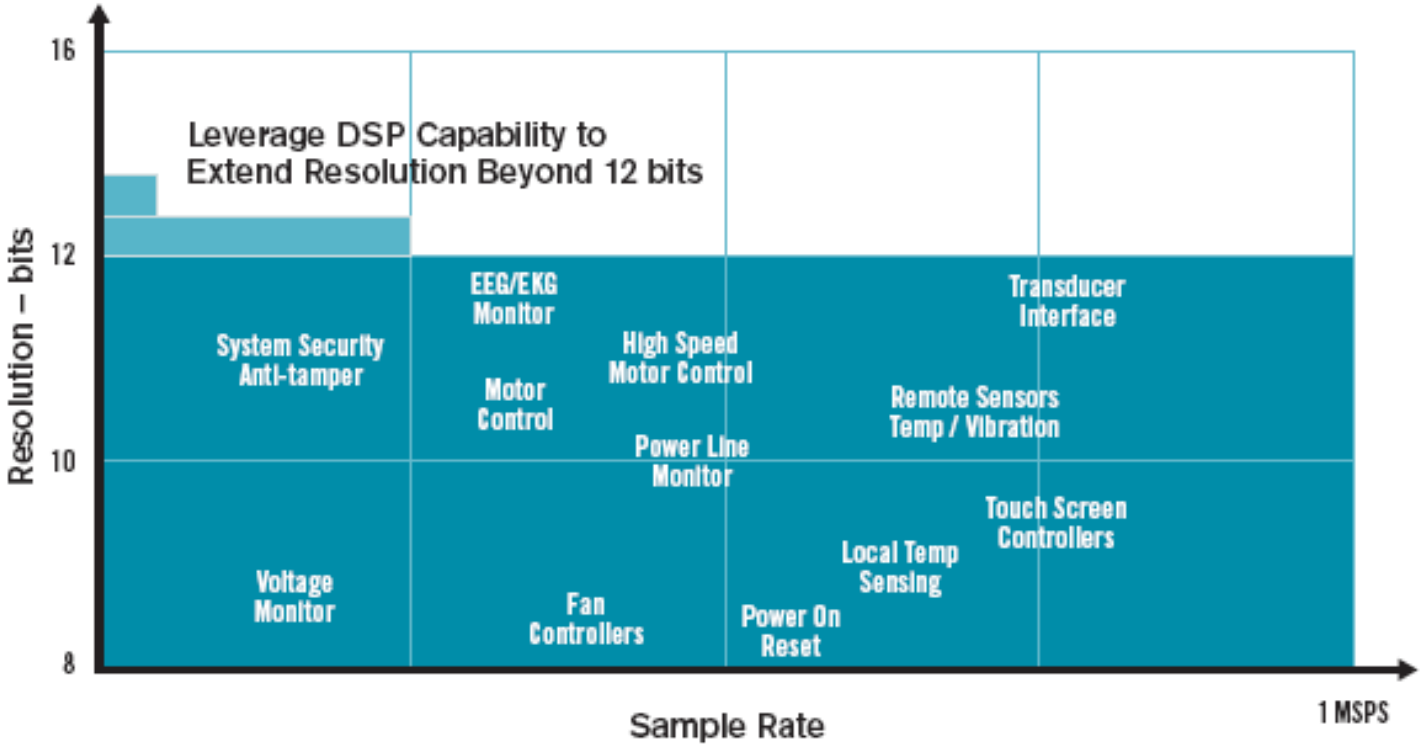
Customized Analog with FPGA Flexibility

- **Significant cost & area savings by integrating common analog functionality**
  - $3+ discrete analog functions integrated
  - General purpose 12-bit Analog Front End covers wide range of General Purpose Analog Applications
- **Customized Analog beyond off-the-shelf Products**
  - Implement simple analog monitoring or
  - Complex analog signal conditioning and processing
- **Enhanced Reliability, Safety, Security**
  - Single chip
  - On-Chip temp & Voltage sensor
- **Available in all 7 series devices**



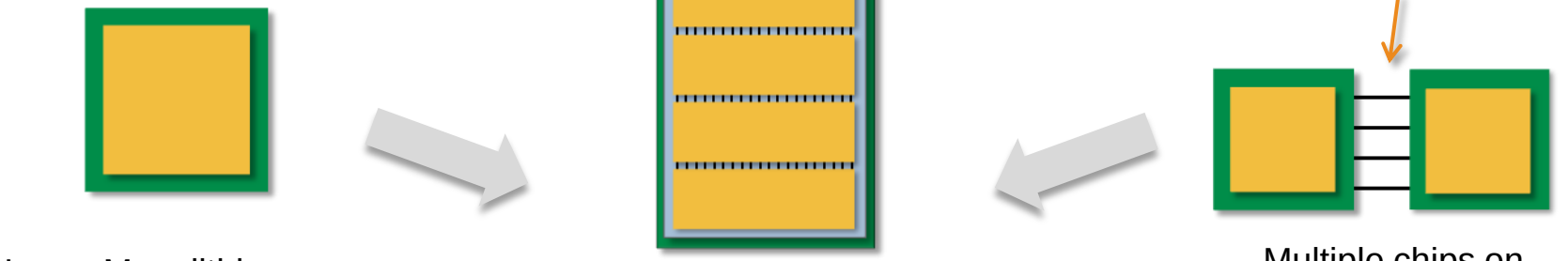
Agile Mixed Signal Technology Applications

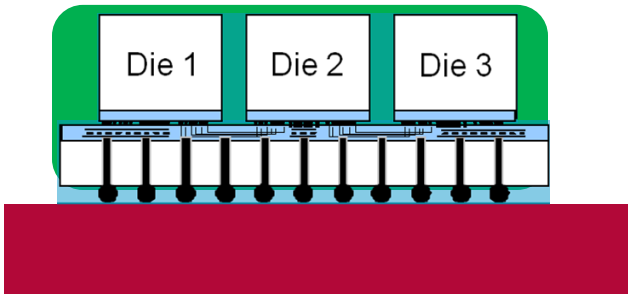
- **XADC specifications cover a wide range of Data Converter applications**
  - Wide range of sampling and timing modes
  - Accommodates various analog signal types



Introducing Stacked Silicon Interconnect Technology

High Bandwidth, Low Latency, Low Power

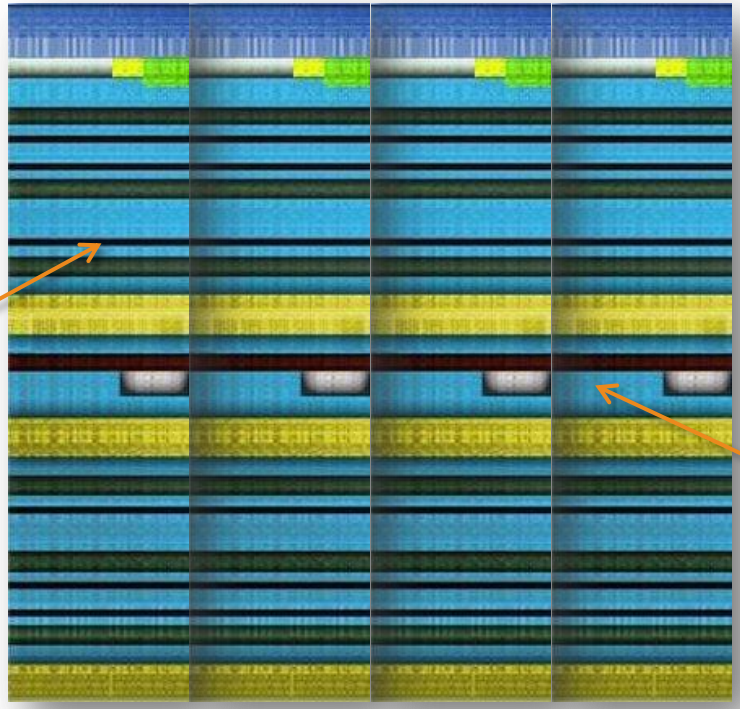




- ✓ Tens of thousands of low latency, die-to-die connections
- ✓ Large devices available earlier in time
- ✓ No wasted I/O power
- ✓ Over five years of R&D

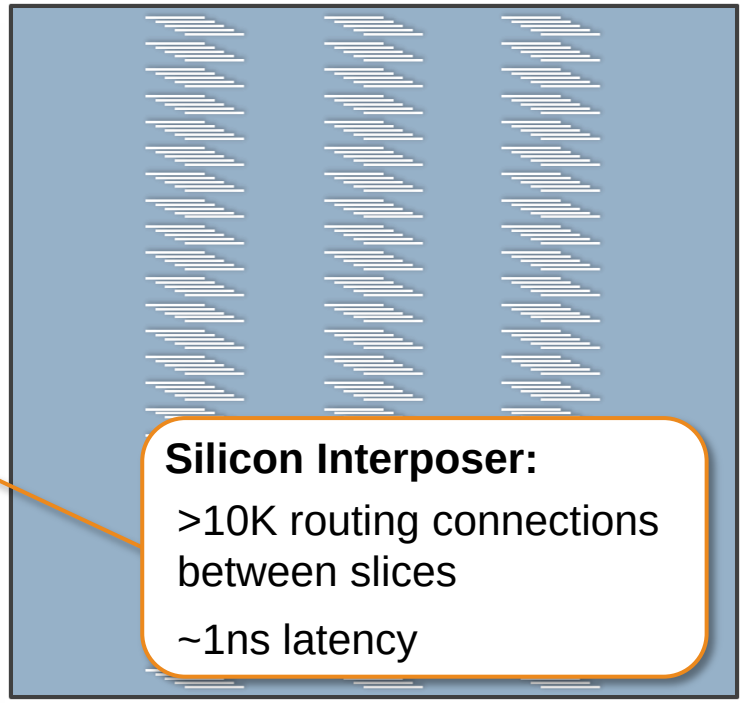
Delivers the Best of Both Worlds: High and Usable Capacity

Xilinx FPGA Architectural Innovations
At the Heart of the Technology



ASMBL Optimized FPGA slice

FPGA Slices Side-by-Side



Silicon Interposer:

>10K routing connections between slices

~1ns latency

Silicon Interposer

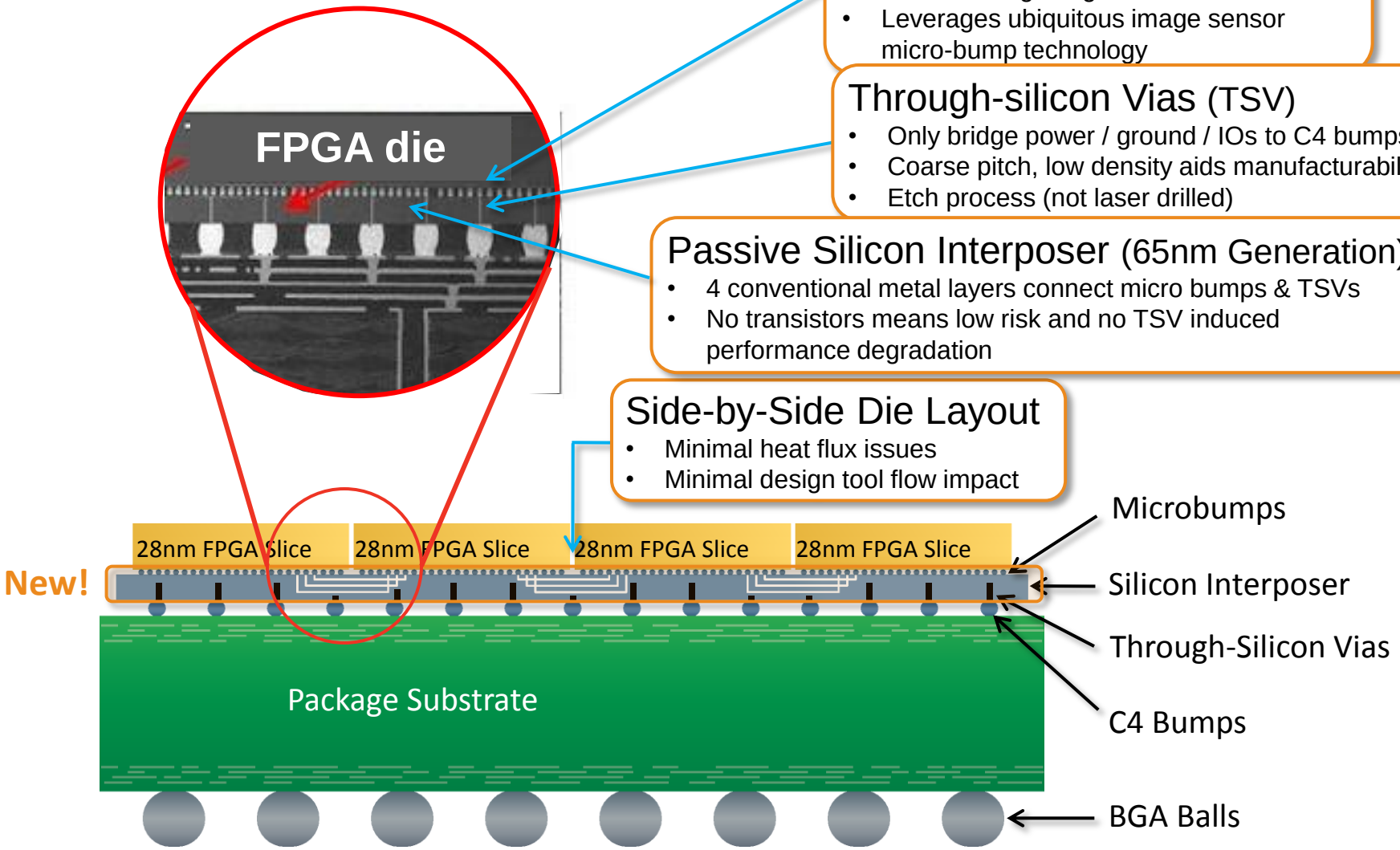
Harnesses Proven Technology in a Unique Way

Microbumps
- Access to power / ground / IOs
- Access to logic regions
- Leverages ubiquitous image sensor micro-bump technology

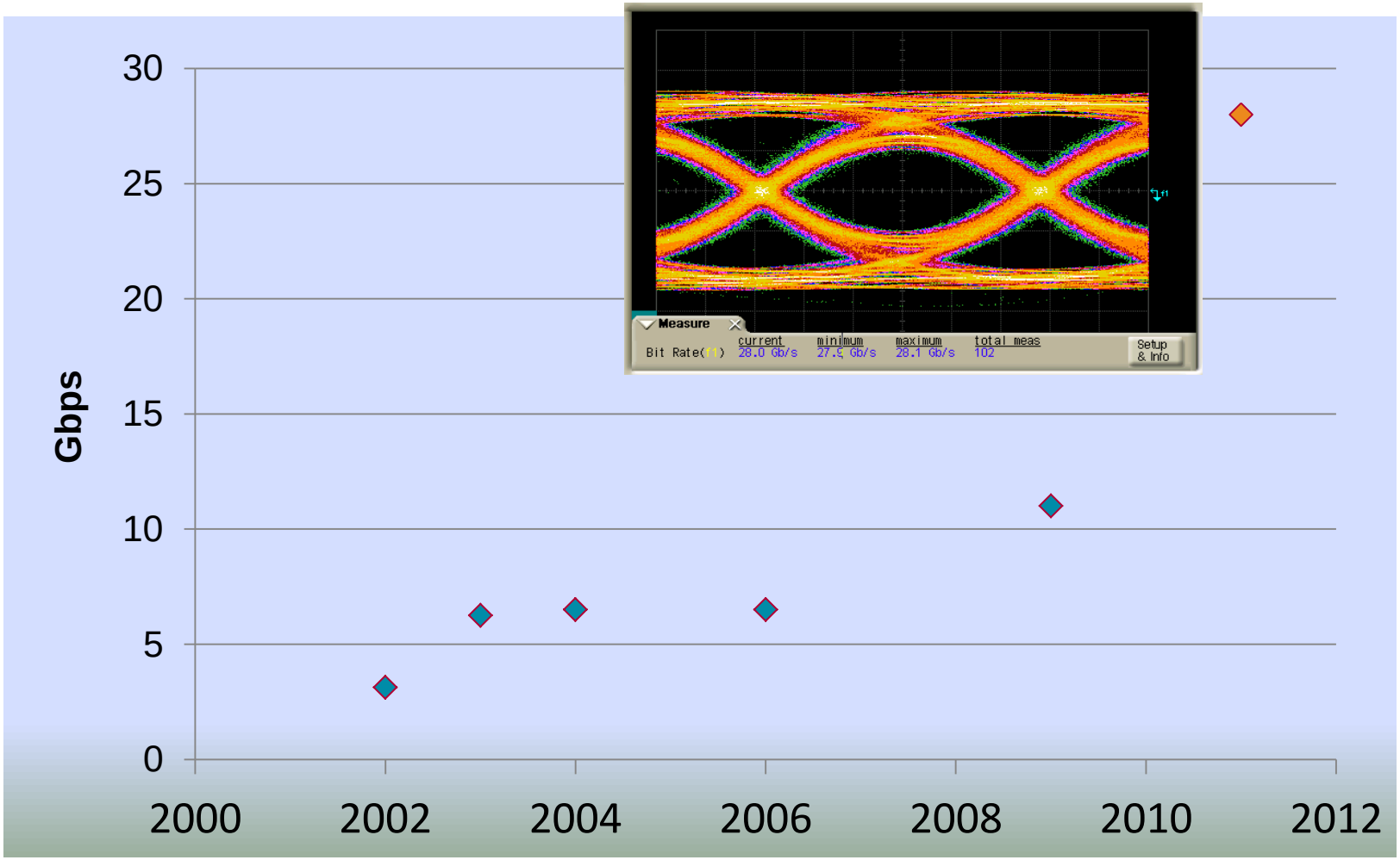
Through-silicon Vias (TSV)
- Only bridge power / ground / IOs to C4 bumps
- Coarse pitch, low density aids manufacturability
- Etch process (not laser drilled)

Passive Silicon Interposer (65nm Generation)
- 4 conventional metal layers connect micro bumps & TSVs
- No transistors means low risk and no TSV induced performance degradation

Side-by-Side Die Layout
- Minimal heat flux issues
- Minimal design tool flow impact

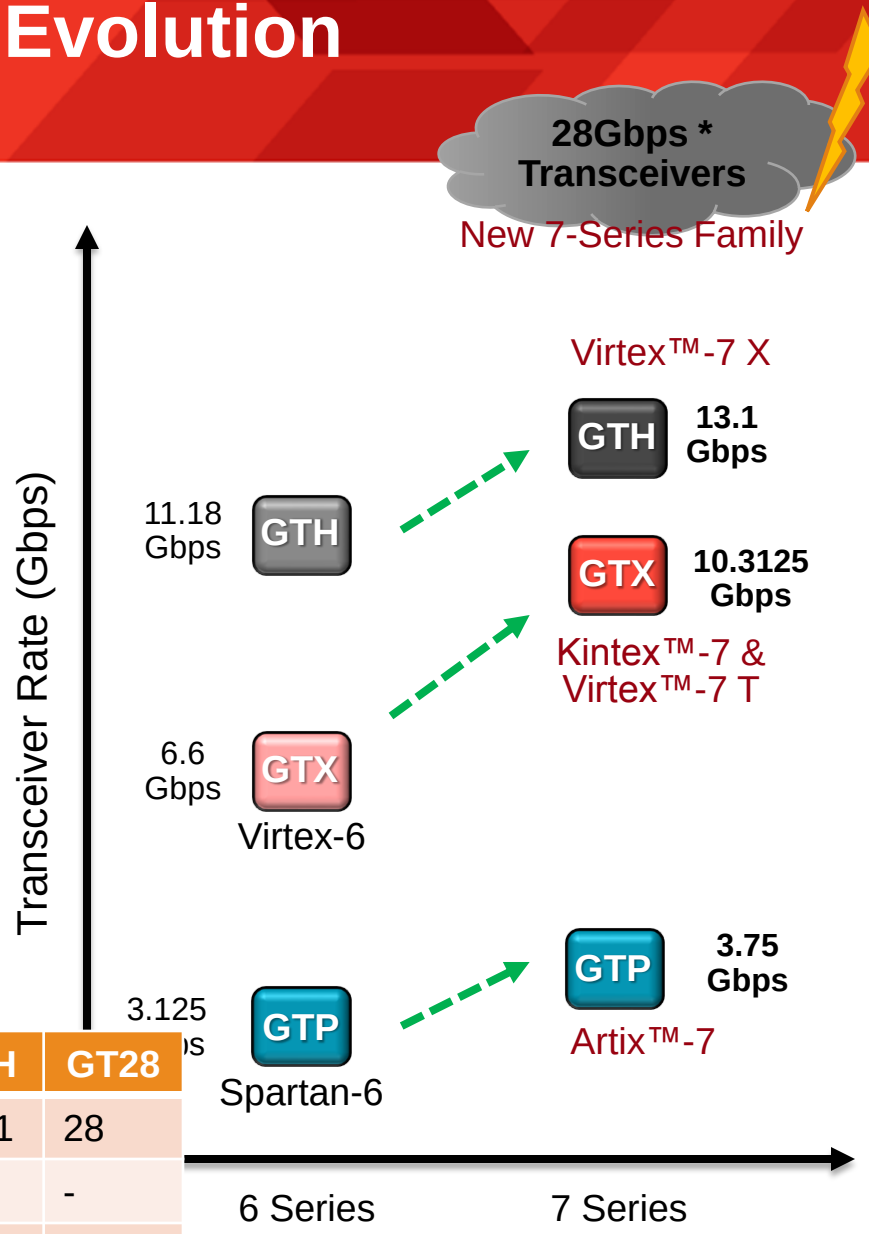


Transceiver Speed Expands Rapidly



High-Speed Transceiver Evolution

- **Challenge:**
  - Increase device BW
  - No increase in total device power
  - XCVR gains from scaling: negligible
- **Solution:**
  - Careful circuit design throughout XCVR
  - Increased Gbps / XCVR
  - More XCVR / Device
  - Low power mode for short channels
  - Lanes share a PLL vs PLL per lane
- **Result:**
  - 60% Increased max device BW
  - Device XCVR power unchanged



	GTP	GTX	GTH	GT28
Max Rate (Gbps)	3.75	10.3125	13.1	28
Relative Power (Per GT)	0.35x	0.7x	1x	-
Max GTs per Device	4	56	72	-

University of Edinburgh
Smith-Waterman DNA Matching

Performance per $

Platform	Performance (MCUPS*) per $ spent	Normalised Performance per $ spent
FPGA	0.34	4.6
GPU	0.14	1.9
Cell BE	0.17	2.3
GPP	0.07	1

Mega Cell Updates Per Second

Performance per Watt

Platform	Performance (MCUPS) per Watt	Normalised Performance per Watt
FPGA	508	584
GPU	22	25
Cell BE	27	31
GPP	0.87	1

Emphasis added

University of Edinburgh
Monte-Carlo Financial Options Pricing

Performance per $

Platform	Performance (Paths/sec) per $ spent	Normalised Performance per $ spent
FPGA	3399	32:1
GPU	3339	32:1
GPP	105	1:1

Performance per Watt

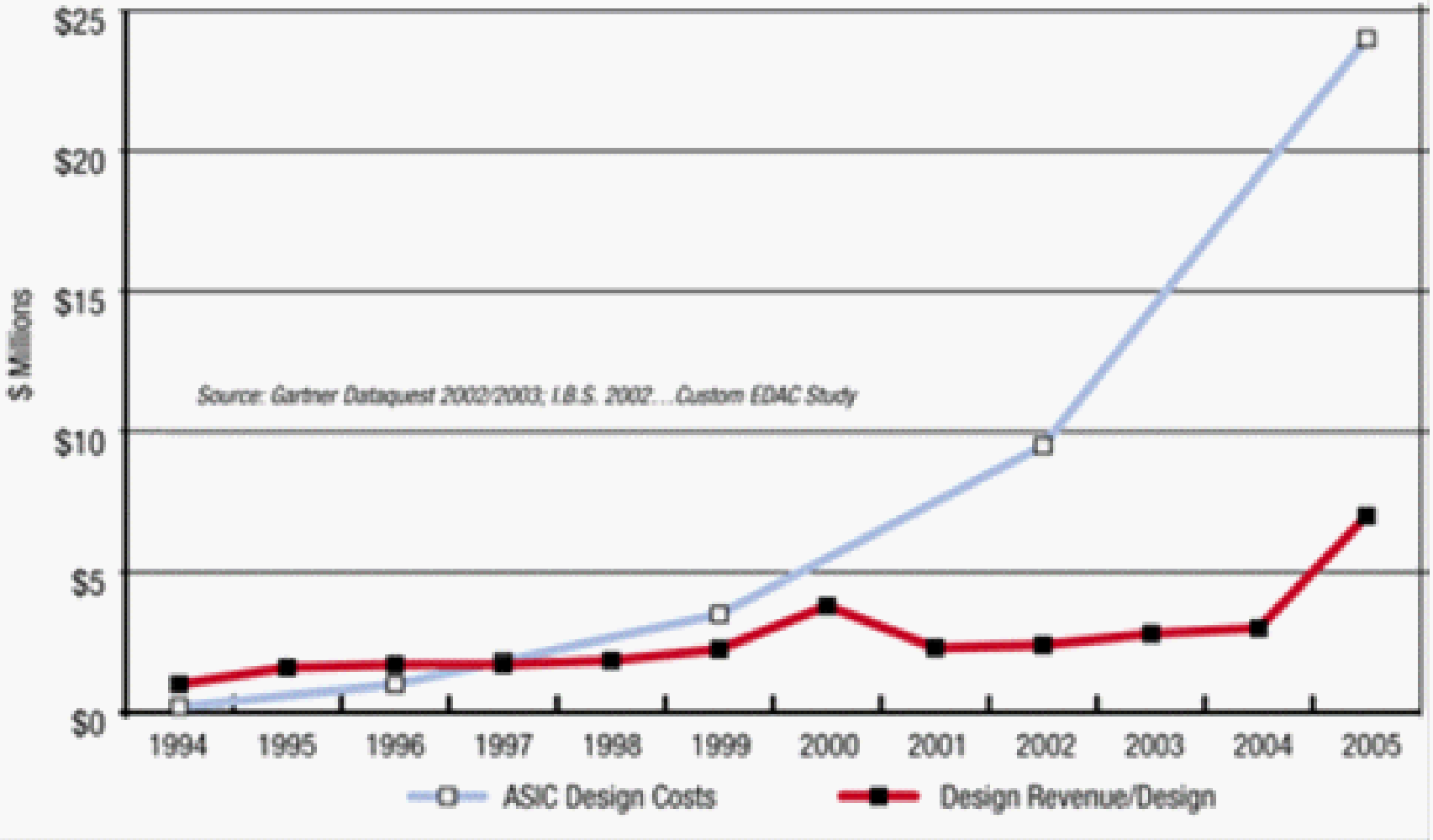
Platform	Paths per Second Per Watt	Normalised Performance per Watt
FPGA	3,330,928	1090:1
GPU	64,322	21:1
GPP	3,055	1:1

The University of Edinburgh, Institute of Integrated Systems, System Level Integration Group

k.benkrid@ieee.org 24th International Conference on Supercomputing, June 1-4, 2010, Tsukuba, Japan Slide 24

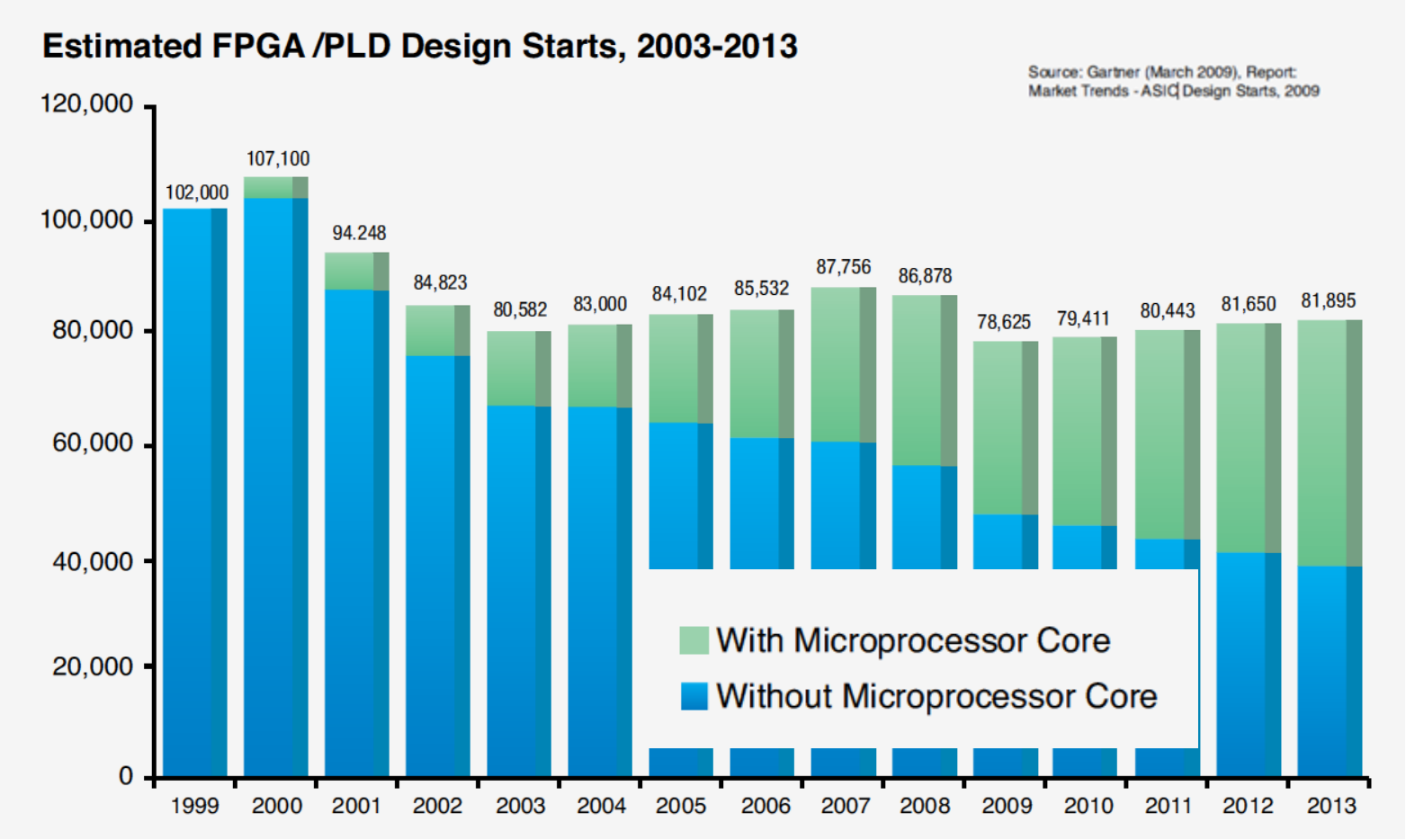
Emphasis added

Design Costs Grow Exponentially, Too



http://www.design-reuse.com

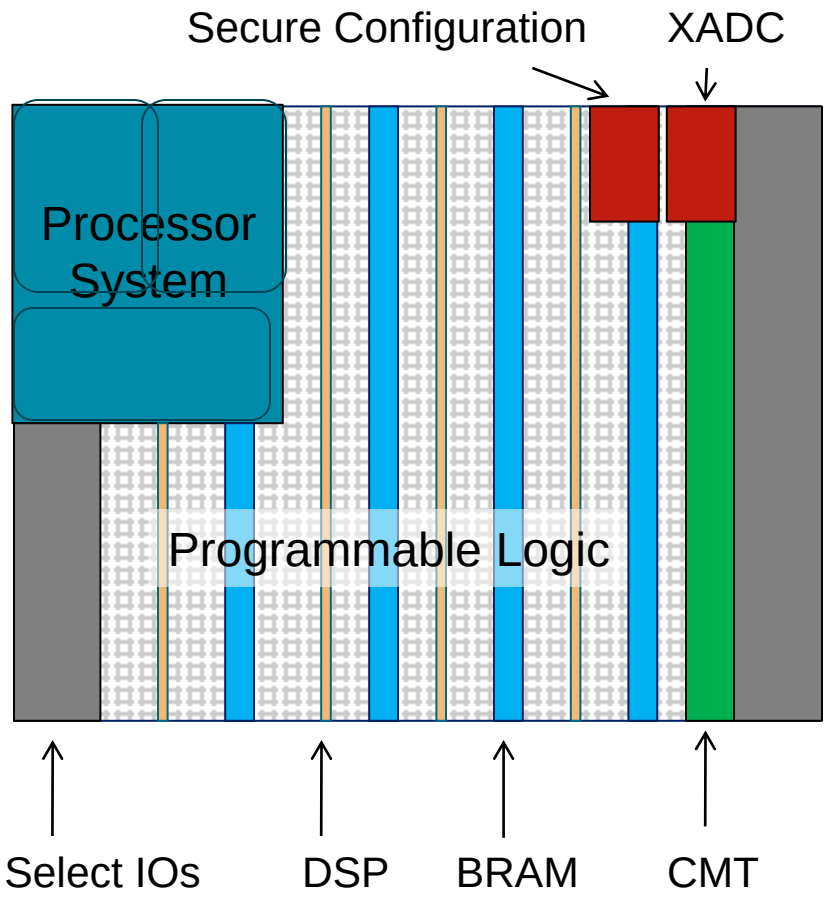
Hardware and Software Programmability



Zynq-7020 Device

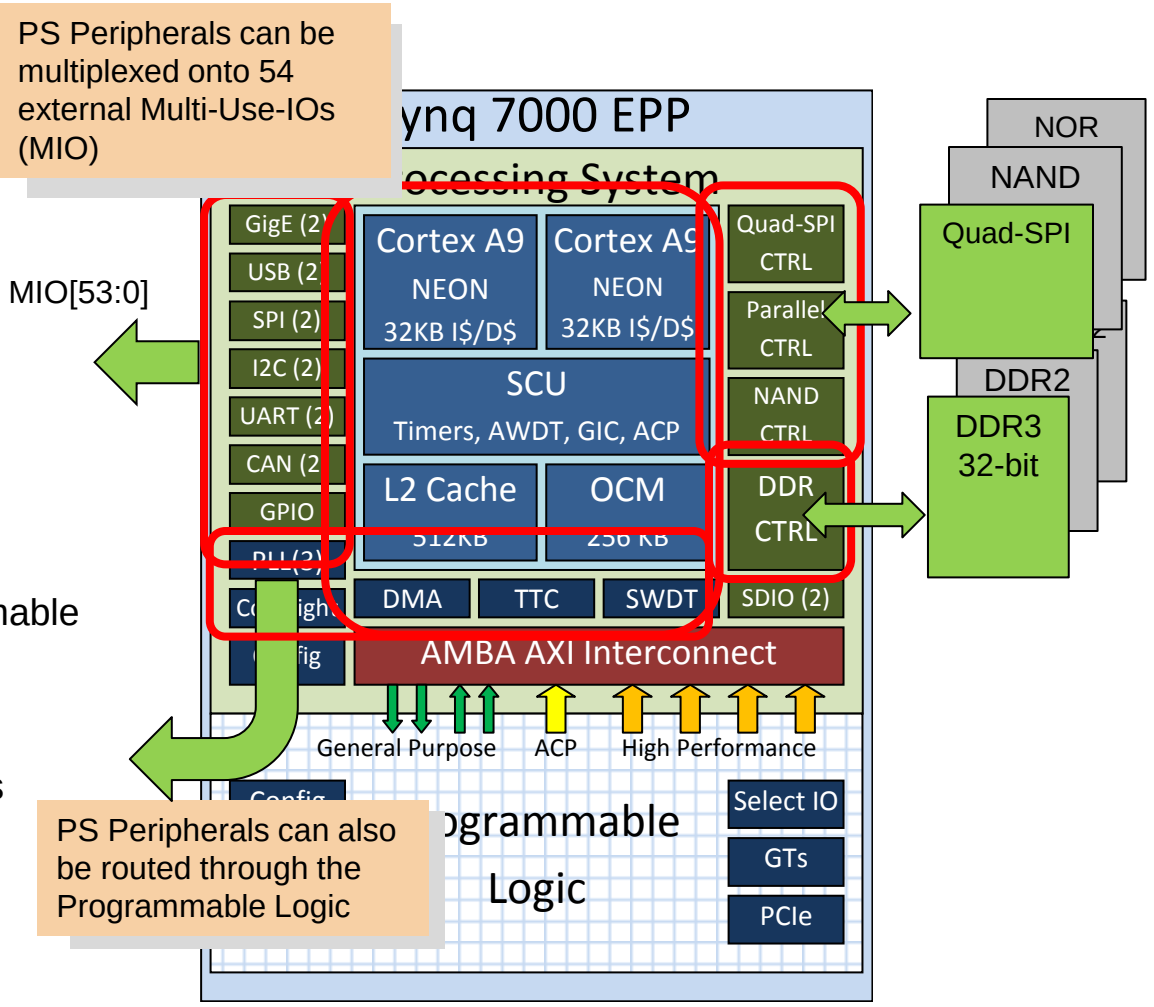
Dual-Core ARM with FPGA Peripheral

- **Processor System (PS)**
  - ARM Cortex-A9 MPcore
  - Standard Peripherals
  - 32-bit DDR3 / LPDDR2 controller
  - 54 Multi-Use IOs
  - 73 DDR IOs
- **Programmable Logic (PL)**
  - 85 K Logic Cells
  - 106K FFs
  - 140 32-Kb Block RAM
  - 220 DSP Blocks
  - Dual 12-bit ADC
  - Secure configuration engine
  - 4 Clock Management Tiles
  - 200 Select IO (1.2-3.3V)



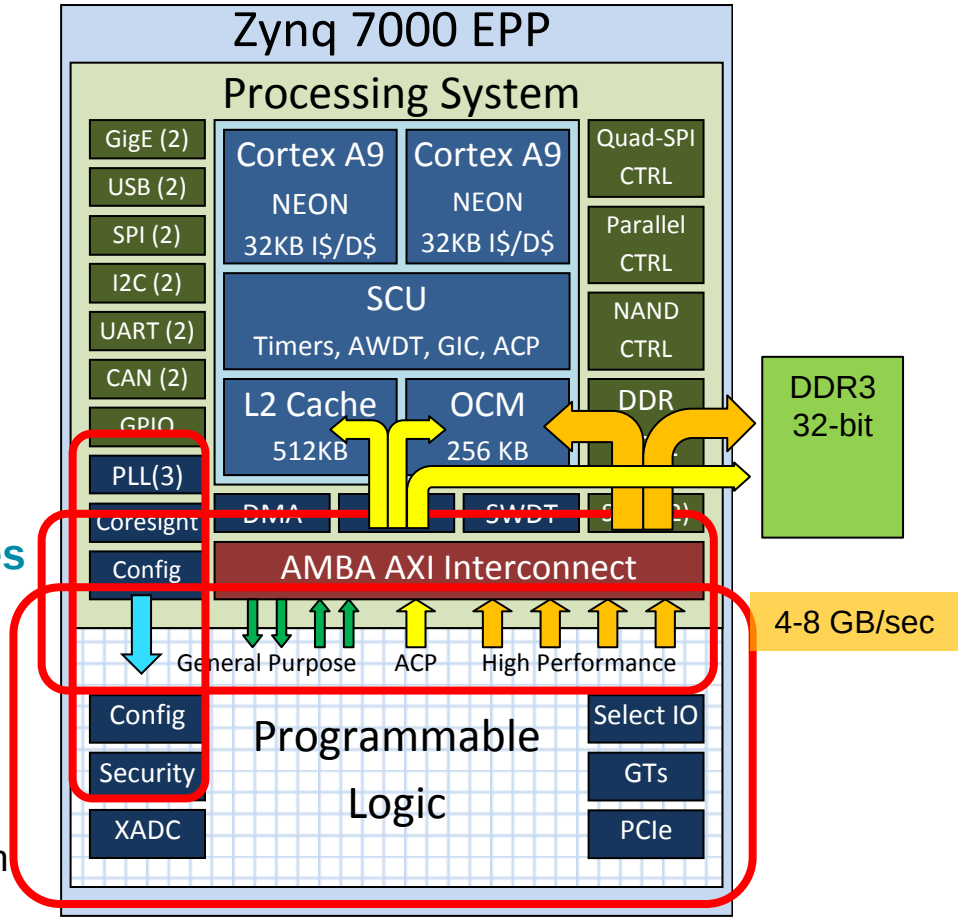
Zynq-7000 Processor System (PS)

- **Dual Core Cortex ARM A9**
  - NEON, 512 KB L2 cache
  - 256 KB On-Chip-Memory (OCM)
- **DDR Interface**
  - DDR3 Performance
  - High BW utilization
- **Config & Legacy Memory I/F**
  - Quad-SPI, NOR, NAND
- **Standard Peripherals – GigE …**
  - Available to PS IO or to Programmable Logic
- **System Level Peripherals**
  - Clock generation, Counter Timers
  - 8 Channel DMA controller
  - Coresight Debugging



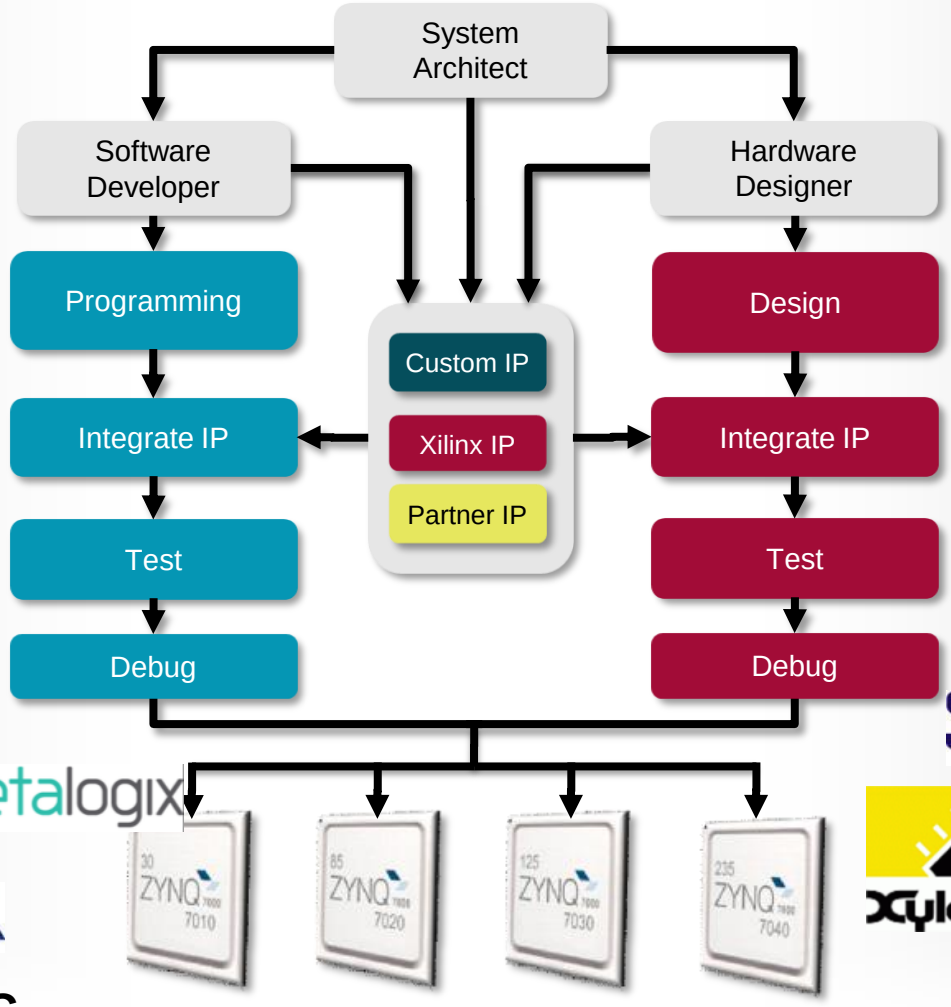
Zynq-7000 Programmable Logic (PL)

- **Programmable Logic Resources**
  - 30K – 235 K Logic Cells
  - Dedicated 36 K-bit BRAMs, DSP, CMT
  - XADC dual channel 12-bit ADC
  - Up to 12 GTs with PCIe hard core
  - Up to 300 Select IOs
- **Programmable Logic AXI Interfaces**
  - Multiple 32/64 bit AXI interfaces to PL
  - Accelerator Coherency Port (ACP) with access to caches
- **Programmable Logic System Interfaces**
  - Interrupts, DMA control
  - Debug
- **High Performance PL Configuration**
  - Security Decryption Engine
  - Under 200 ms configuration time from flash
  - Debugging interfaces



Embedded Design Flow Using Zynq-7000

- **Industry-Leading Tools**
  - Xilinx SDK
  - ARM Ecosystem
- **Many Sources of SW IP**
  - Standardized around AMBA-AXI
  - Xilinx, ARM libraries
  - 3rd Parties

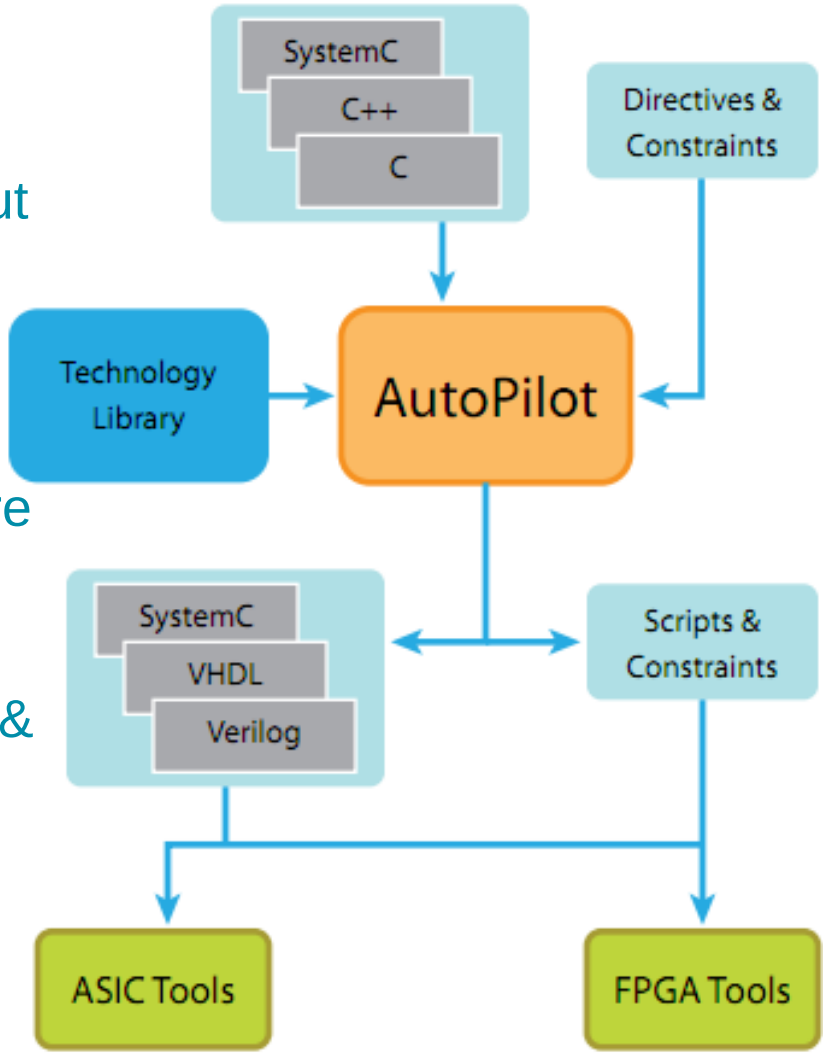


- **Industry-Leading Tools**
  - C-Gates / AutoESL
  - System Generator
  - VHDL/Verilog
- **Many Sources of HW IP**
  - Standardized around AXI
  - 3rd Parties

Xilinx AutoPilot C to Gates

- In 2010, BDTI optical flow benchmark showed quality of output comparable to manual design.

"In our test of Man vs. Machine; Machine won hands down! We were able to create and verify complex matrix inverse in 5 days vs. 3 months; Algorithm to FPGA speed & QoR is unbelievable. If I did not verify in hardware I would think the tool is lying. " —*MilAero Company*

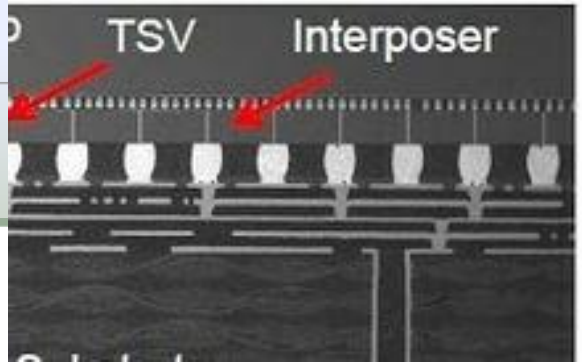


FPGA Leadership at 28nm

- **Lowest Total Power FPGAs**
  - HPL process proven 50% lower over alternative
- **Highest Productivity FPGAs**
  - Unified, plug and play with extensive Ecosystem
  - Agile Mixed Signal (AMS) providing analog capability in all 7 series family members
  - Fastest cost reduction path with EasyPath™-7 (all Virtex-7 FPGAs)
- **Highest Performance FPGAs**
  - Largest capacity: 2M logic cells (XC7V2000T)
  - Largest transceiver count: 96 (XC7VX1140T)
  - 100x better connectivity/watt: Stacked Silicon Interconnect Technology
  - Fastest memory interface: 1,866 Mb/s (Kintex-7 and Virtex-7 FPGAs)
  - Largest Block RAM capacity: 68 Mb (XC7VX1140T)
  - Highest DSP performance: 5,112 GMACS - symmetric mode (XC7VX980T)
- **Innovative Architecture Breaks the Rules**
  - Extensible Processing Platform (Zynq-7000 EPP family)

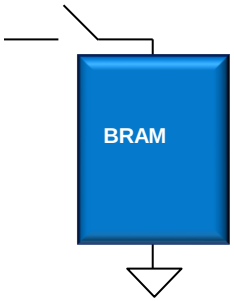
Looking Ahead: Technology

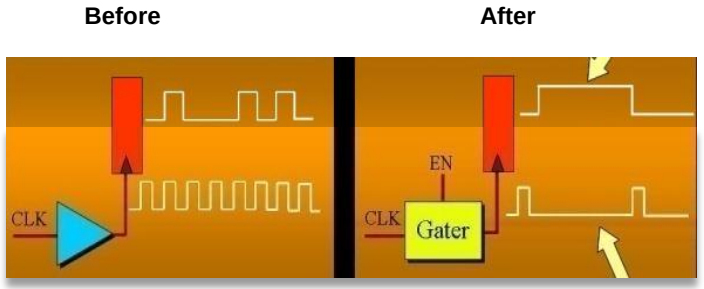
- Moore's Law still operates
- Wafer fabrication delivers more transistors
- Wafer fabrication does not deliver significantly higher clock rate, lower power or bandwidth
- Stacked silicon packaging addresses internal bandwidth and allows further system integration



Looking Ahead: Power

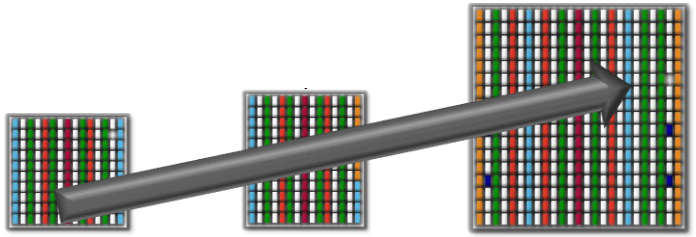
- There is a fundamental tradeoff between performance and power
- The power issue will not go away
- The invisible and easy power optimizations have been done
- Next-generation power management will require thoughtful system design
- Watch for “dark silicon”





Looking Ahead: Design

- The need for efficient design will continue to increase
- More explicit effort on design reuse
- We are raising the design abstraction. Can it get higher than C?
- Specialty languages
- System-oriented devices for major business areas

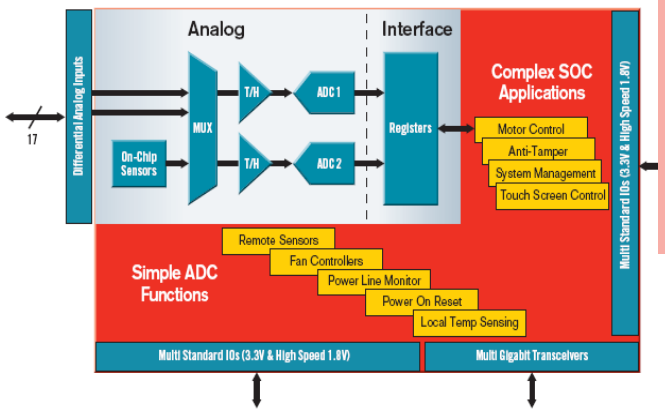


```
void core (
  int n,          // input size
  float *data_in1, // input stream
  float *data_in2, // input stream
  float *data_out // output stream
) {

  int i, j=0;

  for (i=0; i<n; i++)
    data_out[i] = data_in1[i] + data_in2[i];

}
```



Key Messages

- **Still Pushing IC Manufacturing Technology**
  - Programmable logic has been successful because of effective use of Moore's Law
  - Integrated circuit manufacturing doesn't give us all we need
  - More than Moore: 3D, circuits for power, rad-hard, integration
- **Xilinx 7-Series is Pretty Impressive**
  - Capacity, power, I/O bandwidth, processor integration, ADC
  - Xilinx targets its major markets: communications, computing, image processing, automotive, industrial control
- **Power: its Importance Continues to Grow**
  - FPGAs still give the best ops/watt
- **Design Effort**
  - Improved devices, architecture and software


Thank You