Programmable Logic in the 21st Century
Where are we and Where are we going?

Steve Trimberger, Xilinx Fellow
Key Messages

- **Still Pushing IC Manufacturing Technology**
  - Programmable logic has been successful because of effective use of Moore’s Law
  - Integrated circuit manufacturing doesn’t give us all we need
  - More than Moore: 3D, circuits for power, rad-hard, integration

- **Xilinx 7-Series is Pretty Impressive**
  - Capacity, power, I/O bandwidth, processor integration, ADC
  - Xilinx targets its major markets: communications, computing, image processing, automotive, industrial control

- **Power: its Importance Continues to Grow**
  - FPGAs still give the best ops/watt

- **Design Effort**
  - Improved devices, architecture and software
Introducing Xilinx

- **Worldwide leader in programmable solutions**
  - Founded in 1984
  - $2.31B in revenues in 2010
  - ~3,000 employees worldwide
  - 20,000 customers worldwide

- **Pioneer of the fabless semiconductor model**

- **Inventor of the FPGA**

- **50% PLD market segment share**

- **Worldwide presence, with headquarters in San Jose, CA; Dublin, Ireland and Singapore**

*According to market analyst firm iSuppli Corp.*

Source: [http://www.xilinx.com/company/about.htm](http://www.xilinx.com/company/about.htm)
FPGA Capacity Trends

Year


Largest Xilinx FPGA

Number of LCs

1.00E+02 1.00E+03 1.00E+04 1.00E+05 1.00E+06 1.00E+07
FPGA Performance Trends

Extrapolation from ITRS

Historical FPGA data
FPGA Energy Trends (W / LC MHz)

Driven by lower capacitance and voltage
Pause
Solving Next Generation Design Challenges For All Market Segments

Next Gen Wired Communications

Next Gen Wireless Communications

High Performance Computing

Consumer

Lowest Power and Cost

- Portable/handheld ultrasound
- 3D cameras & camcorders
- D-SLR still cameras
- Software defined radio
- 3DTV
- Portable eReaders
- Automotive Infotainment
- Multifunction printers

Industry’s Best Price-Performance

- Wireless LTE infrastructure
- 10G PON OLT line card
- LED backlit & 3D video displays
- Video-over-IP bridge
- Cellular radio
- Medical & Avionics imaging
- Set top boxes
- Motor control

Industry’s Highest System Performance and Capacity

- 400G & 100G line cards
- 300G Interlaken bridge
- Terabit switch fabric
- 100G OTN
- MUXPONDER
- RADAR
- ASIC emulation
- Test & Measurement

Aerospace & Defense

Test & Measurement

Medical Imaging

Audio Video Broadcast
Major Universal Market Challenges

**Market Challenges**

- **Lower Power**
  - Meeting Legislation and Regulations

- **Higher Performance**
  - System Capacity and Capability

- **Improved Productivity**
  - Reduce Capital and Operating Expenses (OPEX, CAPEX)

**Market Segments Affected**

- Flat Panel/TV, Central Office, Server Farms, Portable Medical, Portable and Wired Consumer
- Wired Infrastructure, 400G Networks, Wireless, Broadcast, Defense
- Wireless, Wired, High Performance Computing

#1 problem from over 300 top customers’ surveyed:
Higher System Performance Impacted by Power Budget Limitations
Xilinx 7 Series Highlights

- **7 Series silicon devices**
  - 28 nm Technology, TSMC HPL process
  - 50% reduction in power over 40 nm devices

- **3 FPGA Fabrics**
  - Artix = Low cost, low power FPGA ("1W FPGA")
  - Kintex = Density & performance FPGA ("Market Sweet spot")
  - Virtex = Highest density and performance FPGA ("More than Moore")

- **‘More than Moore’ density increase**
  - Up to 2M logic cells
  - Using Stacked Silicon Interconnect Technology (SSIT)

- **Improved GT bandwidth**
  - GT bandwidth increased to 28 GHz

- **Zynq Embedded Processing Platform (EPP)**
Ground Breaking Capacity Gains at 28nm
World’s First 2 Million Logic Cell FPGA

- Over 2x capacity increases over Spartan-6 and Virtex-6 FPGAs

<table>
<thead>
<tr>
<th>Family</th>
<th>Capacity Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARTIX-7</td>
<td>8K – 350K LCs</td>
</tr>
<tr>
<td>KINTEX-7</td>
<td>70K – 480K LCs</td>
</tr>
<tr>
<td>VIRTEX-7</td>
<td>330K – 2M LCs</td>
</tr>
</tbody>
</table>

- 8K – 2M LCs; the widest capacity range offered in a single unified product family

- Larger densities enable higher performance
  - More calculations/clock cycle by utilizing parallelism inherent in FPGAs
Unified Architecture Boosts Design Productivity
Accelerating Design Creation, Debug and Simplifying Reuse

Unified HW Architecture

Unified SW Architecture

Plug & Play IP

Plug & Play Boards

Processor

AXI Interconnect Block

DMA

AXI DDR3 Mem Ctrl

TEMAC

AXI4 (data)

AXI4 Lite

AXI4 Liter

AXI4 Liter

AXI4 Liter

AXI4 Liter

XST
ngdbuild
map
par
trce
bitgen
Coregen
EDK
SysGen
3rd party
Rodin
Pre-verified IP assembly tool

Plug & Play Boards
High-k Metal Gate Transistor Rescues Moore’s Law

The Transistor Re-Invented

HKMG:
- introduced by Intel at 45nm
- available at 28nm from top foundries

> 25x lower gate oxide leakage
> 30% lower switching power
> 30% higher drive current or
> 5x lower source-drain leakage

7 Series Power Efficiency Focus from Every Angle

Additional Power Saving Features

Integrated Analog Front End

Design Green

Reducing Static Power

High performance, low power process

Transistor choice optimization

BRAM

Unused BRAM Power Savings

Reducing Dynamic Power

Process Shrink

Reducing I/O Power

Optimized Hard Blocks

IO Design & User Power Saving Modes

-2L Xilinx 7 Series FPGAs

Reducing I/O Power

Fine grain clock and logic gating

Lower device core voltage

5th gen. partial reconfiguration
Xilinx History of Systems Integration

1986
- Oscillator
- Distributed RAM
- Block RAM
- Dual Port RAM
- CMOS / TTL Programmable I/O
- I/O Buffers with Programmable Drive Strength
- Multi-Standard Programmable I/O Support
- Phase Locked Loops
- I/O Termination Impedance
- DSP
- LVDS Transceivers
- Processor
- Multi-Gigabit SerDes
- Phase Multi-Mode Clock Generators
- Mixed Signal System Monitor
- PCI Interface
- Ethernet MAC

2000

2011
- Stacked Silicon Interconnect
- Agile Mixed Signal Converter
- Extensible Processing Sub-system

System Power
BOM Cost
System Performance
Agile Mixed Signal (AMS) Technology
Customized Analog with FPGA Flexibility

- **Significant cost & area savings by integrating common analog functionality**
  - $3+ discrete analog functions integrated
  - General purpose 12-bit Analog Front End covers wide range of General Purpose Analog Applications

- **Customized Analog beyond off-the-shelf Products**
  - Implement simple analog monitoring or
  - Complex analog signal conditioning and processing

- **Enhanced Reliability, Safety, Security**
  - Single chip
  - On-Chip temp & Voltage sensor

- **Available in all 7 series devices**
XADC specifications cover a wide range of Data Converter applications

- Wide range of sampling and timing modes
- Accommodates various analog signal types
Introducing Stacked Silicon Interconnect Technology
High Bandwidth, Low Latency, Low Power

Large Monolithic FPGA

Xilinx Innovation

- Tens of thousands of low latency, die-to-die connections
- Large devices available earlier in time
- No wasted I/O power
- Over five years of R&D

I/O performance bottlenecks & power

Multiple chips on PCB or MCB

Delivers the Best of Both Worlds: High and Usable Capacity
Xilinx FPGA Architectural Innovations
At the Heart of the Technology

ASMBL Optimized FPGA slice

FPGA Slices Side-by-Side

Silicon Interposer:
>10K routing connections between slices
~1ns latency
Harnesses Proven Technology in a Unique Way

Microbumps
- Access to power / ground / IOs
- Access to logic regions
- Leverages ubiquitous image sensor micro-bump technology

Through-silicon Vias (TSV)
- Only bridge power / ground / IOs to C4 bumps
- Coarse pitch, low density aids manufacturability
- Etch process (not laser drilled)

Passive Silicon Interposer (65nm Generation)
- 4 conventional metal layers connect micro bumps & TSVs
- No transistors means low risk and no TSV induced performance degradation

Side-by-Side Die Layout
- Minimal heat flux issues
- Minimal design tool flow impact

New!
- Minimal heat flux issues
- Minimal design tool flow impact
Transceiver Speed Expands Rapidly
High-Speed Transceiver Evolution

- **Challenge:**
  - Increase device BW
  - No increase in total device power
  - XCVR gains from scaling: negligible

- **Solution:**
  - Careful circuit design throughout XCVR
  - Increased Gbps / XCVR
  - More XCVR / Device
  - Low power mode for short channels
  - Lanes share a PLL vs PLL per lane

- **Result:**
  - 60% Increased max device BW
  - Device XCVR power unchanged

<table>
<thead>
<tr>
<th></th>
<th>GTP</th>
<th>GTX</th>
<th>GTH</th>
<th>GT28</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Rate (Gbps)</td>
<td>3.75</td>
<td>10.3125</td>
<td>13.1</td>
<td>28</td>
</tr>
<tr>
<td>Relative Power (Per GT)</td>
<td>0.35x</td>
<td>0.7x</td>
<td>1x</td>
<td>-</td>
</tr>
<tr>
<td>Max GTs per Device</td>
<td>4</td>
<td>56</td>
<td>72</td>
<td>-</td>
</tr>
</tbody>
</table>
### Performance per $ $

<table>
<thead>
<tr>
<th>Platform</th>
<th>Performance (MCUPS*) per $ spent</th>
<th>Normalised Performance per $ spent</th>
</tr>
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<tbody>
<tr>
<td>FPGA</td>
<td>0.34</td>
<td>4.6</td>
</tr>
<tr>
<td>GPU</td>
<td>0.14</td>
<td>1.9</td>
</tr>
<tr>
<td>Cell BE</td>
<td>0.17</td>
<td>2.3</td>
</tr>
<tr>
<td>GPP</td>
<td>0.07</td>
<td>1</td>
</tr>
</tbody>
</table>

*Mega Cell Updates Per Second

### Performance per Watt

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<th>Platform</th>
<th>Performance (MCUPS) per Watt</th>
<th>Normalised Performance per Watt</th>
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<tbody>
<tr>
<td>FPGA</td>
<td>508</td>
<td>584</td>
</tr>
<tr>
<td>GPU</td>
<td>22</td>
<td>25</td>
</tr>
<tr>
<td>Cell BE</td>
<td>27</td>
<td>31</td>
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<tr>
<td>GPP</td>
<td>0.87</td>
<td>1</td>
</tr>
</tbody>
</table>

The University of Edinburgh, Institute of Integrated Systems, System Level Integration Group

k.benkrid@ieee.org  24th International Conference on Supercomputing, June 1-4, 2010, Tsukuba, Japan  Slide 17
### Performance per $

<table>
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<tr>
<td>FPGA</td>
<td>3399</td>
<td>32:1</td>
</tr>
<tr>
<td>GPU</td>
<td>3339</td>
<td>32:1</td>
</tr>
<tr>
<td>GPP</td>
<td>105</td>
<td>1:1</td>
</tr>
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</table>

### Performance per Watt

<table>
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<th>Platform</th>
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</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>3,330,928</td>
<td>1090:1</td>
</tr>
<tr>
<td>GPU</td>
<td>64,322</td>
<td>21:1</td>
</tr>
<tr>
<td>GPP</td>
<td>3,055</td>
<td>1:1</td>
</tr>
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</table>
Design Costs Grow Exponentially, Too

http://www.design-reuse.com
Hardware and Software Programmability

Estimated FPGA/PLD Design Starts, 2003-2013

Source: Gartner (March 2009), Report: Market Trends - ASIC Design Starts, 2009

- With Microprocessor Core
- Without Microprocessor Core
**Processor System (PS)**
- ARM Cortex-A9 MPcore
- Standard Peripherals
- 32-bit DDR3 / LPDDR2 controller
- 54 Multi-Use IOs
- 73 DDR IOs

**Programmable Logic (PL)**
- 85 K Logic Cells
- 106K FFs
- 140 32-Kb Block RAM
- 220 DSP Blocks
- Dual 12-bit ADC
- Secure configuration engine
- 4 Clock Management Tiles
- 200 Select IO (1.2-3.3V)
Zynq-7000 Processor System (PS)

- **Dual Core Cortex ARM A9**
  - NEON, 512 KB L2 cache
  - 256 KB On-Chip-Memory (OCM)

- **DDR Interface**
  - DDR3 Performance
  - High BW utilization

- **Config & Legacy Memory I/F**
  - Quad-SPI, NOR, NAND

- **Standard Peripherals – GigE ...**
  - Available to PS IO or to Programmable Logic

- **System Level Peripherals**
  - Clock generation, Counter Timers
  - 8 Channel DMA controller
  - Coresight Debugging

PS Peripherals can be multiplexed onto 54 external Multi-Use-I/Os (MIO)

PS Peripherals can also be routed through the Programmable Logic
Programmable Logic Resources
- 30K – 235 K Logic Cells
- Dedicated 36 K-bit BRAMs, DSP, CMT
- XADC dual channel 12-bit ADC
- Up to 12 GTs with PCIe hard core
- Up to 300 Select IOs

Programmable Logic AXI Interfaces
- Multiple 32/64 bit AXI interfaces to PL
- Accelerator Coherency Port (ACP) with access to caches

Programmable Logic System Interfaces
- Interrupts, DMA control
- Debug

High Performance PL Configuration
- Security Decryption Engine
- Under 200 ms configuration time from flash
- Debugging interfaces
Embedded Design Flow Using Zynq-7000

- **Industry-Leading Tools**
  - Xilinx SDK
  - ARM Ecosystem

- **Many Sources of SW IP**
  - Standardized around AMBA-AXI
  - Xilinx, ARM libraries
  - 3rd Parties

- **Industry-Leading Tools**
  - C-Gates / AutoESL
  - System Generator
  - VHDL/Verilog

- **Many Sources of HW IP**
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- **Design**
  - Programming
  - Integrate IP
  - Test
  - Debug

- **Hardware Designer**
  - Design
  - Integrate IP
  - Test
  - Debug

- **System Architect**
  - Software Developer
  - Integrate IP
  - Xilinx IP
  - Partner IP

- **Software Developer**
  - Custom IP
  - Xilinx IP
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In 2010, BDTI optical flow benchmark showed quality of output comparable to manual design.

“In our test of Man vs. Machine; Machine won hands down! We were able to create and verify complex matrix inverse in 5 days vs. 3 months; Algorithm to FPGA speed & QoR is unbelievable. If I did not verify in hardware I would think the tool is lying. “ — MilAero Company
FPGA Leadership at 28nm

- **Lowest Total Power FPGAs**
  - HPL process proven 50% lower over alternative

- **Highest Productivity FPGAs**
  - Unified, plug and play with extensive Ecosystem
  - Agile Mixed Signal (AMS) providing analog capability in all 7 series family members
  - Fastest cost reduction path with EasyPath™-7 (all Virtex-7 FPGAs)

- **Highest Performance FPGAs**
  - Largest capacity: 2M logic cells *(XC7V2000T)*
  - Largest transceiver count: 96 *(XC7VX1140T)*
  - 100x better connectivity/watt: Stacked Silicon Interconnect Technology
  - Fastest memory interface: 1,866 Mb/s *(Kintex-7 and Virtex-7 FPGAs)*
  - Largest Block RAM capacity: 68 Mb *(XC7VX1140T)*
  - Highest DSP performance: 5,112 GMACS - symmetric mode *(XC7VX980T)*

- **Innovative Architecture Breaks the Rules**
  - Extensible Processing Platform (Zynq-7000 EPP family)
Looking Ahead: Technology

- Moore’s Law still operates
- Wafer fabrication delivers more transistors
- Wafer fabrication does not deliver significantly higher clock rate, lower power or bandwidth
- Stacked silicon packaging addresses internal bandwidth and allows further system integration
Looking Ahead: Power

- There is a fundamental tradeoff between performance and power
- The power issue will not go away
- The invisible and easy power optimizations have been done
- Next-generation power management will require thoughtful system design
- Watch for “dark silicon”
Looking Ahead: Design

- The need for efficient design will continue to increase
- More explicit effort on design reuse
- We are raising the design abstraction. Can it get higher than C?
- Specialty languages
- System-oriented devices for major business areas

```c
void core (  
    int n,  // input size  
    float *data_in1, // input stream  
    float *data_in2, // input stream  
    float *data_out // output stream  
) {
    int i, j=0;
    for (i=0; i<n; i++)
        data_out[i] = data_in1[i] + data_in2[i];
}
```
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Thank You