First measurement of single event upsets in the readout control FPGA of the ALICE TPC detector

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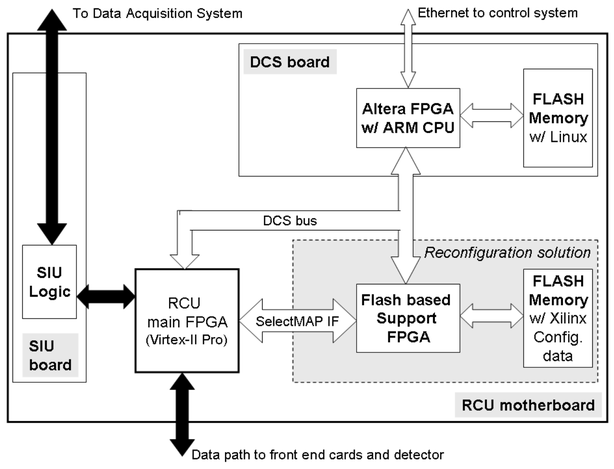
Abstract

Measurements of Single Event Upsets (SEUs) in the configuration memory of the readout control FPGA in the ALICE TPC detector have been performed during stable beam conditions in the period from May to August 2011.

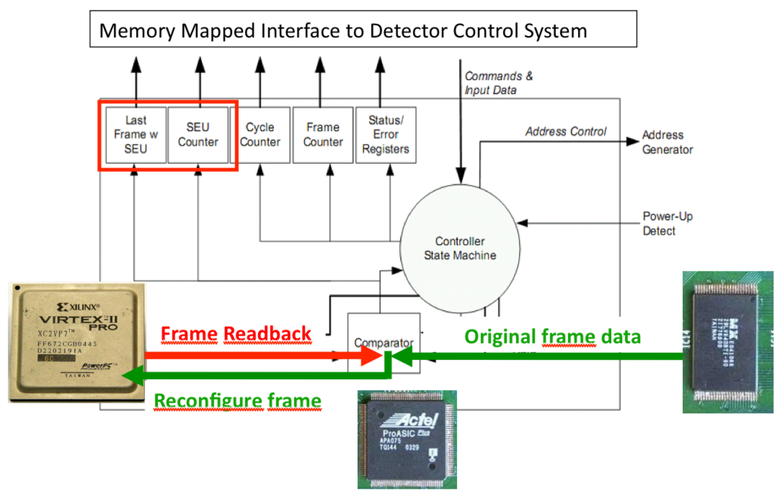
SEU reconfiguration & monitoring

The Readout Control Unit (RCU)



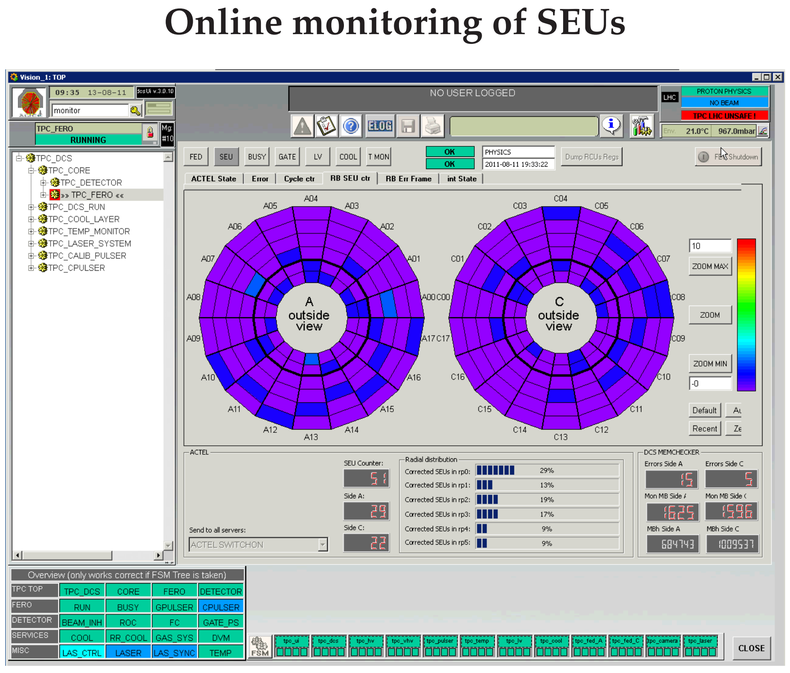
The main components of the recofiguration solution are the radiation tolerant Flash based support FPGA from Actel [5] (the reconfiguration controller), and a Flash memory device for storage of original configuration data. The support FPGA can be remotely controlled through the Detector Control System (DCS) [6].

Readback and reconfiguration



By continuously reading back the configuration memory of the RCU main FPGA, an SEU is detected by comparing the read back data to the original data stored in the Flash memory. If different, the corrupt part of the configuration memory is reconfigured with the correct data. The solution is based on partial reconfiguration which allows to reconfigure a subset of the configuration memory without interrupting the operation of the RCU main FPGA [7].

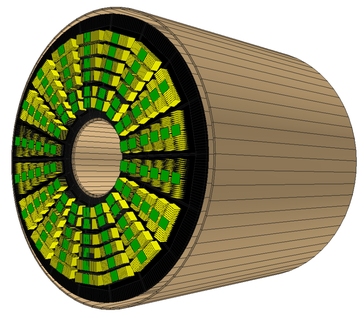
Online monitoring of SEUs



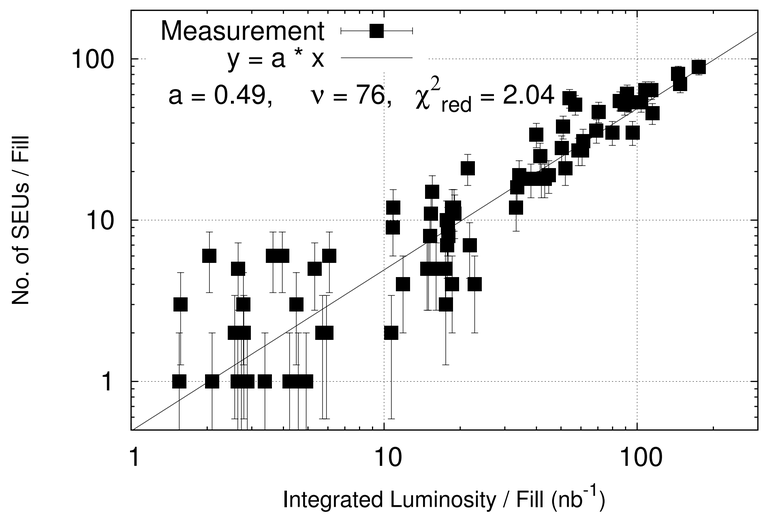
A dedicated user interface has been implemented using PVSSII [8]. It provides online monitoring of the reconfiguration solution and the number of detected and corrected SEUs.

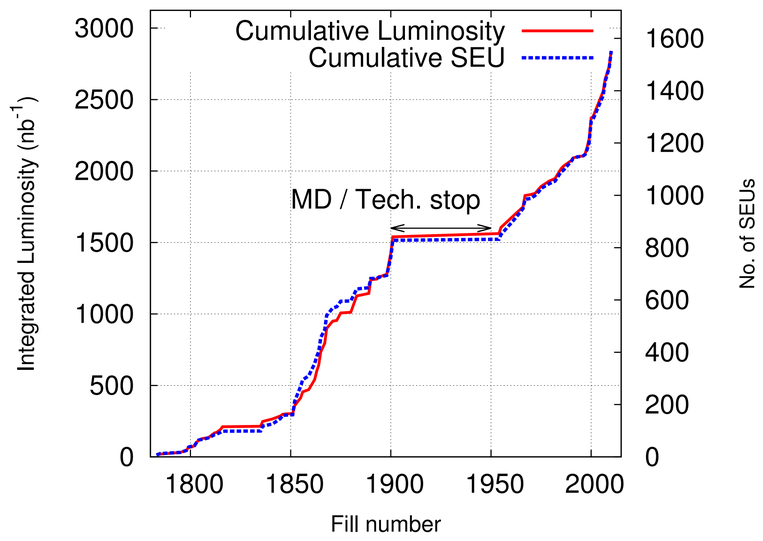
Introduction

- The Time Projection Chamber (TPC)[1] is the main tracking detector of the ALICE experiment[2]. The 18 trapezoidal sectors on each side of the TPC are divided into 6 readout partitions. Each readout partition is controlled by the Readout Control Unit (RCU) (green) which is connected to a number of front-end cards (yellow).
- The RCU is in charge of the data readout for the TPC with the main contol functionality implemented in an SRAM based FPGA from Xilinx. Due to the radiation induced by the colliding proton beams, Single Event Upsets (SEUs) are expected in the configuration memory of this FPGA. A reconfiguration solution has therefore been implemented to detect and correct these SEUs [3],[4].

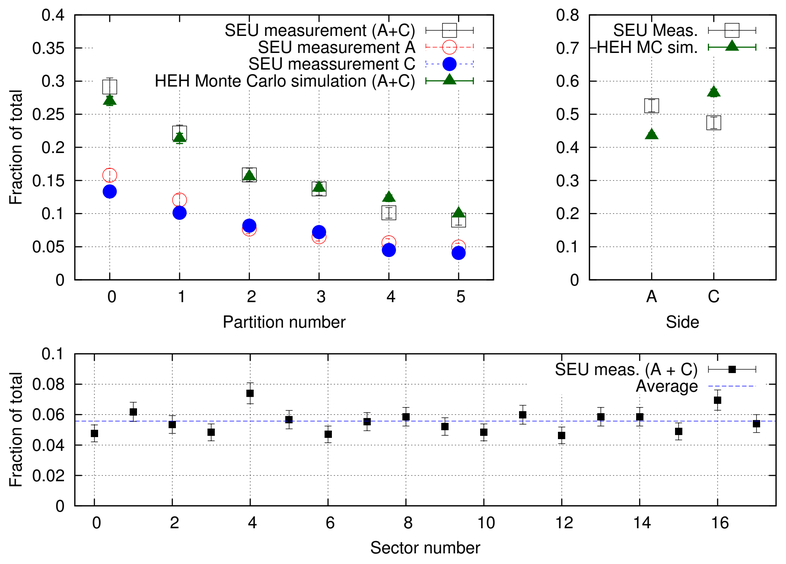


Measurement results

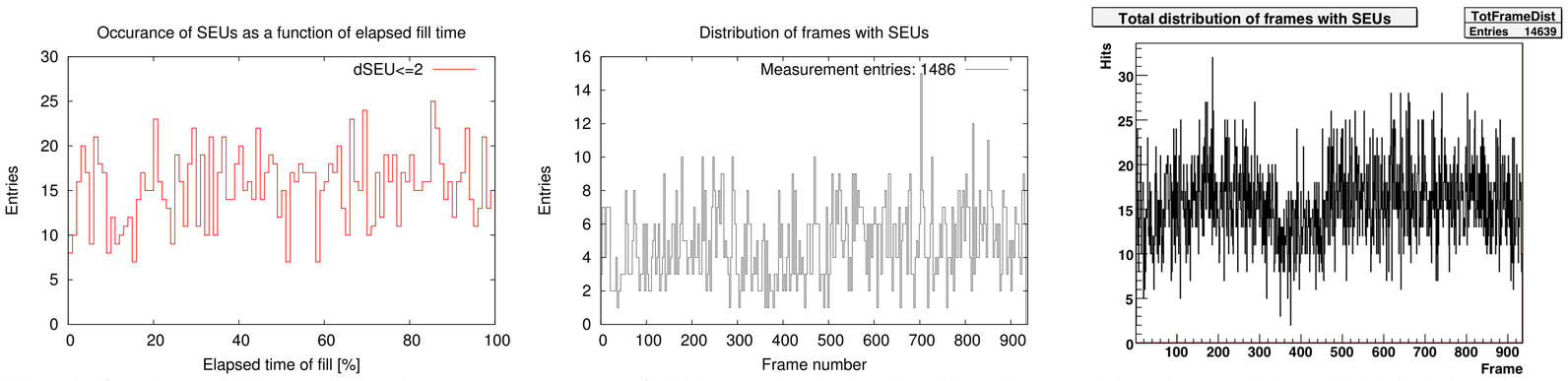




The analysis is based on the integrated luminosity [9] (for fills > 1 nb^{-1}) and number of SEUs accumulated during stable beam conditions for pp collisions at a center-of-mass energy of $\sqrt{s}$ = 7 TeV. In total 1552 SEUs were corrected in the period of May until August (fills 1783 - 2010).



- The number of SEUs in the configuration memory of the FPGA is assumed to be proportional to the fluence of high energy hadrons (HEH) ($\sim >$ 20 MeV).
- A good qualitative agreement is found when comparing the relative radial distribution of measured SEUs to Monte Carlo simulation (PbPb) [3] result of the HEH fluence.
- However, the small asymmetry observed between the A-side and C-side (Muon absorber side) is in contradiction to the simulations results.



The left plot shows that the occurance of SEUs are evenly distributed in time. The SEU bit locations are also evenly distributed (middle) within the configuration memory of the FPGA. This is expected with a uniform exposure of radiation and also seen during irradiation tests (right).

Summary

The measurement results show an linear dependence between the number of SEUs in the configuration memory of the RCU main FPGA and the cumulative integrated luminosity. Approximately 0.5 SEUs can be expected in the system of 216 FPGA per integrated luminosity of 1 nb^{-1} during pp collisions at $\sqrt{s}$ = 7 TeV.

References

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