

## Irradiation of DEPFET-like transistors with CO-60 gamma source up to 10 MRad

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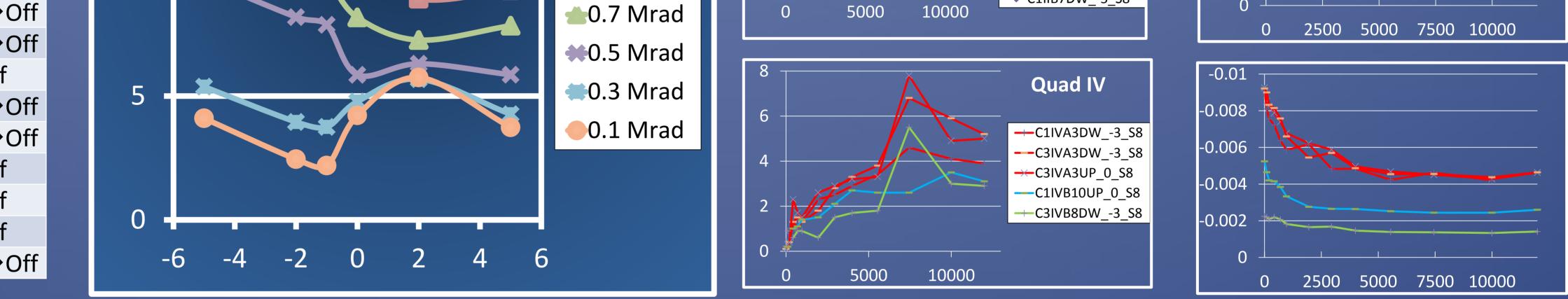
## ABSTRACT

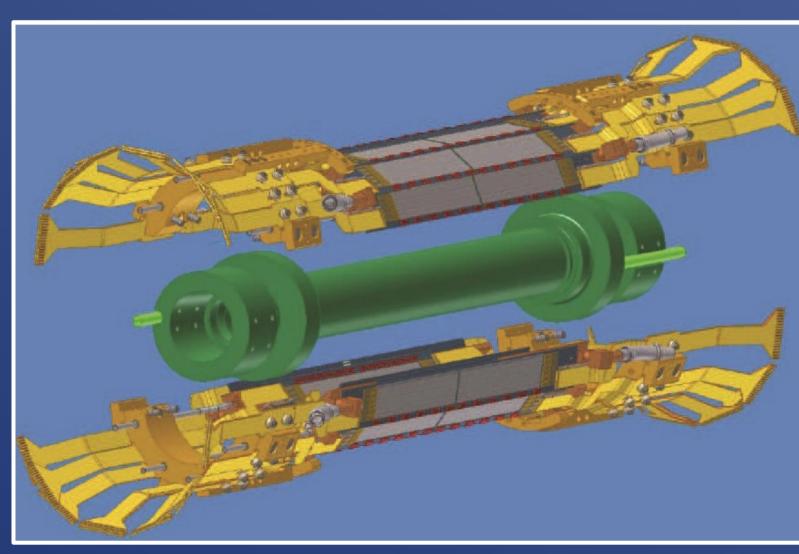
The Pixel Detector (PXD) of the Belle II experiment at superKEKB accelerator in Japan is based in the DEPFET technology. Two layers of 8+12 modules at a radius of 13 and 22 mm will give a spatial resolution below 10  $\mu$ m. The radiation level expected in the first layer in ten years of operation is about 10 MRad of total ionizing dose. In order to study the tolerance of the DEPFET technology sixty devices were irradiated using a standard procedure like <sup>60</sup>Co gamma source. Different doping types, channel sizes and biasing conditions were studied.

## SETUP

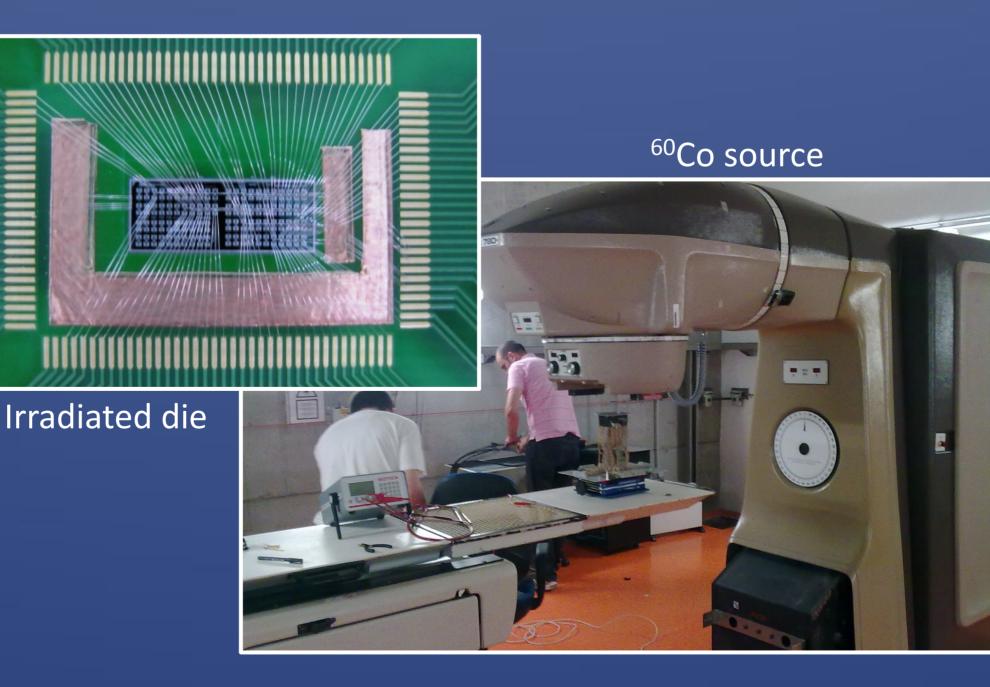
Two dies with 30 devices each of 3 doping types were instrumented. Initially (14, 22, 24) devices of types (QI, QII, QIV) with threshold voltages (3.5V, 0.5V, -2V) were irradiated. Due to different problems, mostly electrostatic discharges during manipulation not related to the irradiation, only 22 of them survived (see table). Threshold voltage shift, gain variation and sub-threshold size were studied with different biasing conditions. The influence of manufacturing and operational parameter such as doping, channel dimension and biasing voltage were studied. The irradiation took place in 11 steps during the summer 2010 in the Radiation Physics Laboratory of the Santiago de Compostela University using a radioactive source of 2080 Ci of activity allowing a dose of 11 krad/h.

	- Threshold voltage shift (V) vs Vgs (V)								s (V)		Subth size (V) vs Irradiation (Krad)		Gain vs Irradiation (Krad)
Туре	Vth0	Transistor	W(um)	Vd	Vg State						<sup>8</sup> Quad I		-0.01
QI	3.5	c2-IB7-1	6	-5	0 On $\rightarrow$ Off	2	5				6C3IA3DW_2_S8		-0.008
		c2-IB8-1	10	-5	0 On $\rightarrow$ Off		👘 🖌 🎽				$\begin{array}{c}\text{C1IA3DW}_2\text{_S8} \\\text{C3IA3UP}_0\text{_S8} \end{array}$		-0.006
		c2-IB10-1	40	-5	0 On $\rightarrow$ Off						—C3IB10UP_0_S8		-0.004
		c1-IA3-2	120	-5	2 On $\rightarrow$ Off		•		🗰 10 Mrad		2C3IB8UP_0_S8 C3IB7UP_0_S8		-0.002
		c2-IA3-1	120	-5	2 On $\rightarrow$ Off	2			₩7.5 Mrad				0
		c2-IA3-2	120	-5	2 On $\rightarrow$ Off						0 5000 10000		0 2500 5000 7500 10000
QII		c1-IIB7-1	6	-5	-1 On →Off			Annealed 		8 Quad II		-0.01	
		c1-IIB7-2	6	-5	-5 On →Off		_		<b>+</b> 5.5 Mrad		6		-0.008
		c2-IIB7-1	6	0	-1 Off	1	5						
		c1-IIB8-2	10	-5	5 Off				-3 Mrad	4	4		-0.006
		c2-IIB8-2	10	0	5 Off						C1IIB9UP1_S8 C1IIB8DW_5_S8		-0.004
	0.5	c1-IIB9-1	20	-5	-1 On →Off	1				2 - 0 - 0	-→-C3IIB8DW_5_S8 -→-C3IIB7UP1_S8		-0.002
		c1-IIB9-2	20	-5	-5 On →Off	1	0		1 Mrad		0  ←C1IIB7UP1_S8		
		c1-IIB10-1	40	-5	-5 On →Off				📥 0.7 Mrad		0 5000 10000 <u>→−C1IIB7DW5_S8</u>		0 2500 5000 7500 10000
		c1-IIB10-2	40	-5	-2 On →Off				₩0.5 Mrad				0 2300 3000 7300 10000
		c2-IIB10-2	40	0	-2 Off		-				8 Quad IV		-0.01
		c1-IIB11-2	80	-5	-5 On →Off		5			6		-0.008	
QIV	-2	c2-IVB8-2	10	-5	-3 On →Off				0.1 Mrad				-0.006
		c1-IVB10-1	40	0	0 Off						4 → C3IVA3UP_0_S8		-0.004
		c1-IVA3-2	120	0	-3 Off		<u> </u>			2	2		
		c2-IVA3-1	120	-5									-0.002
		c2-IVA3-2	120	-5	-3 On →Off		-6 -	-4 -2 0 2 4 6	6		0 5000 10000		0 2500 5000 7500 10000





Pixel detector for Belle II experiment





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**Biasing-Testing setup** 

## SUMMARY

After being irradiated with a gamma source up to 10 MRad, thick oxide DEPFET-like transistors have shown a negative voltage shift of 18-23 V, reduced to 14-20 V after 28 days of annealing at room temperature. This voltage shift is foreseen to be compensated by changing the operation voltage in the switcher, the steering chip used for DEPFET matrix operation. In order to reduce the voltage shift, therefore the complexity of this chip, a new thin oxide technology is currently being developed in the DEPFET collaboration showing promising results in the first tests.

Despite the fact the gain was found to be 5 times lower than expected by the ratio W/L, the gain is reduced by a factor 2 after 10 MRad. The subthreshold size increased from 0.1 V before irradiation up to 2-6 V after the irradiation, released to 3-6 V after the annealing, the increase is proportional to the channel width.

**References:** S. Rummel, L. Andricek NIMA 623 (2010) 189–191