AMC13 Project

Status

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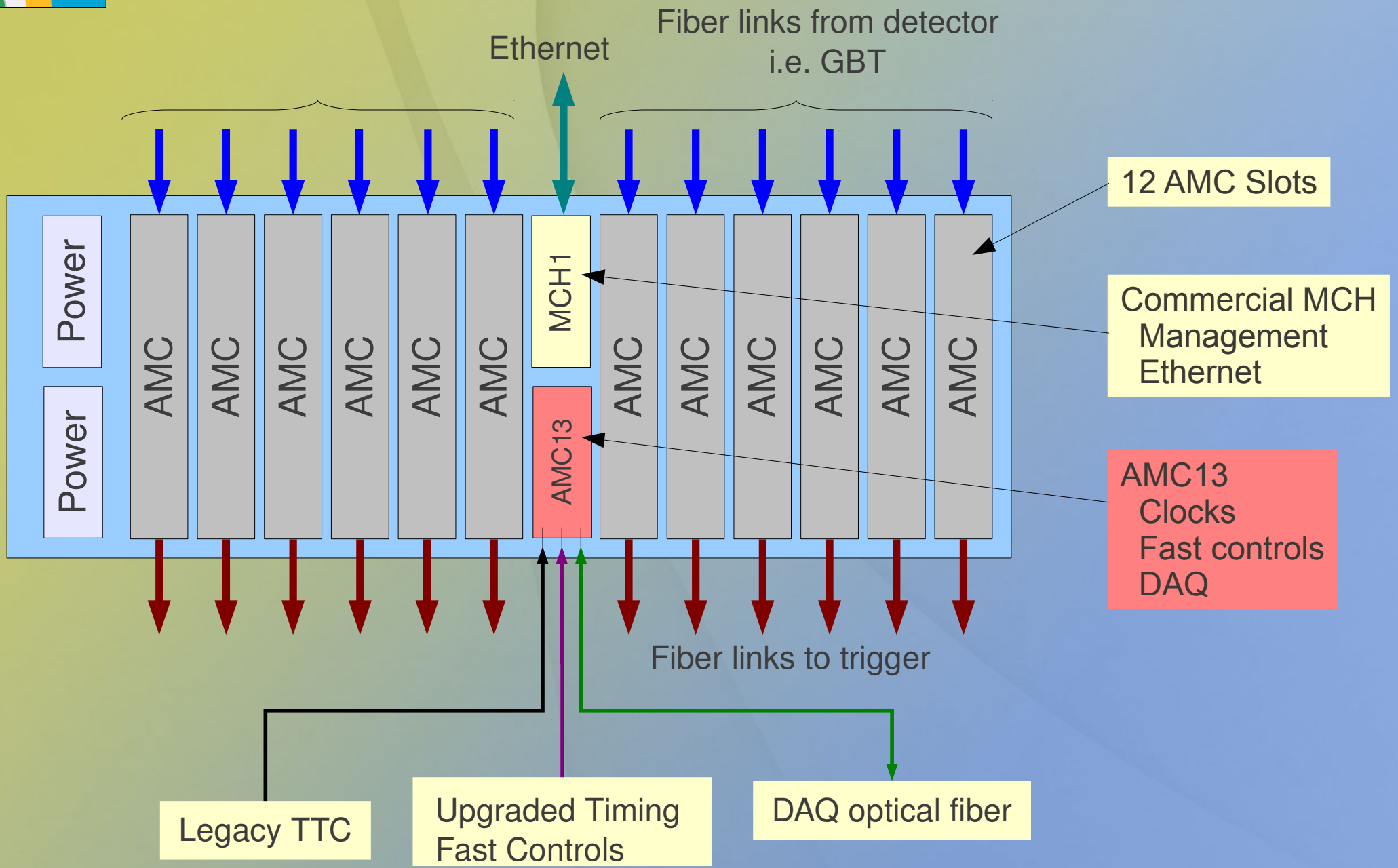
for the CMS Collaboration

What is AMC13?

- It is *not* an MCH! It is a 13th AMC in MCH-2 slot
- It distributes LHC clock / timing / controls to AMCs
- It collects DAQ data from AMCs
- It provides standard interface to CMS subdetectors:
  - CMS DAQ via optical fibers (currently 2 at ~ 6Gb/s)
  - TTC via 1300nm fiber @ 160Mb/sec biphase mark code
    - Future TTC upgrade may be supported via spare SFP site
  - TTS via 1300nm fiber with protocol *t.b.d.*
- It is expected to evolve somewhat to comply with evolving new standards from central services

CMS uTCA Readout Crate (i.e. HCAL)



AMC13 Board Stack

- Base configuration has only tongues 1, 2
- Base board - With optics and HS links (Fabric A)
- Clocks board - distributes LHC clock and controls
- Mezzanine connector for T3 with I2C
  - T3 has JTAG and LEDs

T3 board

Provides JTAG / LEDs on front panel
Can be removed after initial programming

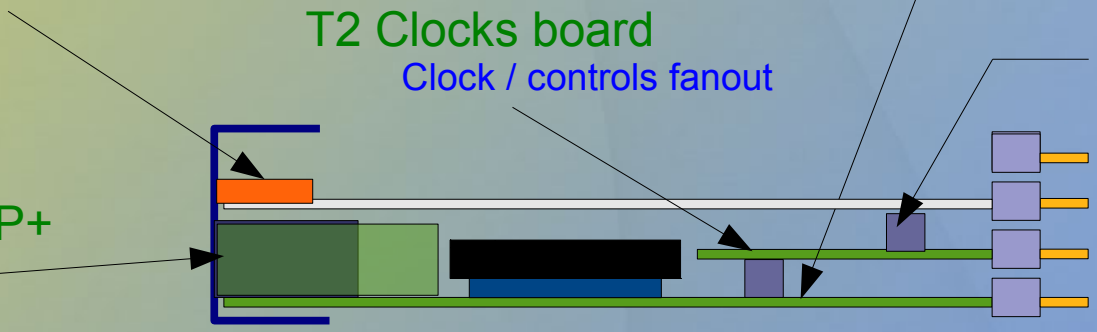
Crosspoint switch or other custom board
can be installed here (but see notes!)

T1 base board

MMC functions (Wisconsin firmware)
TTC optical rx
3x SFP+ cage
Cross-over GbE from MCH1
for controls and local DAQ

T2 Clocks board

Clock / controls fanout

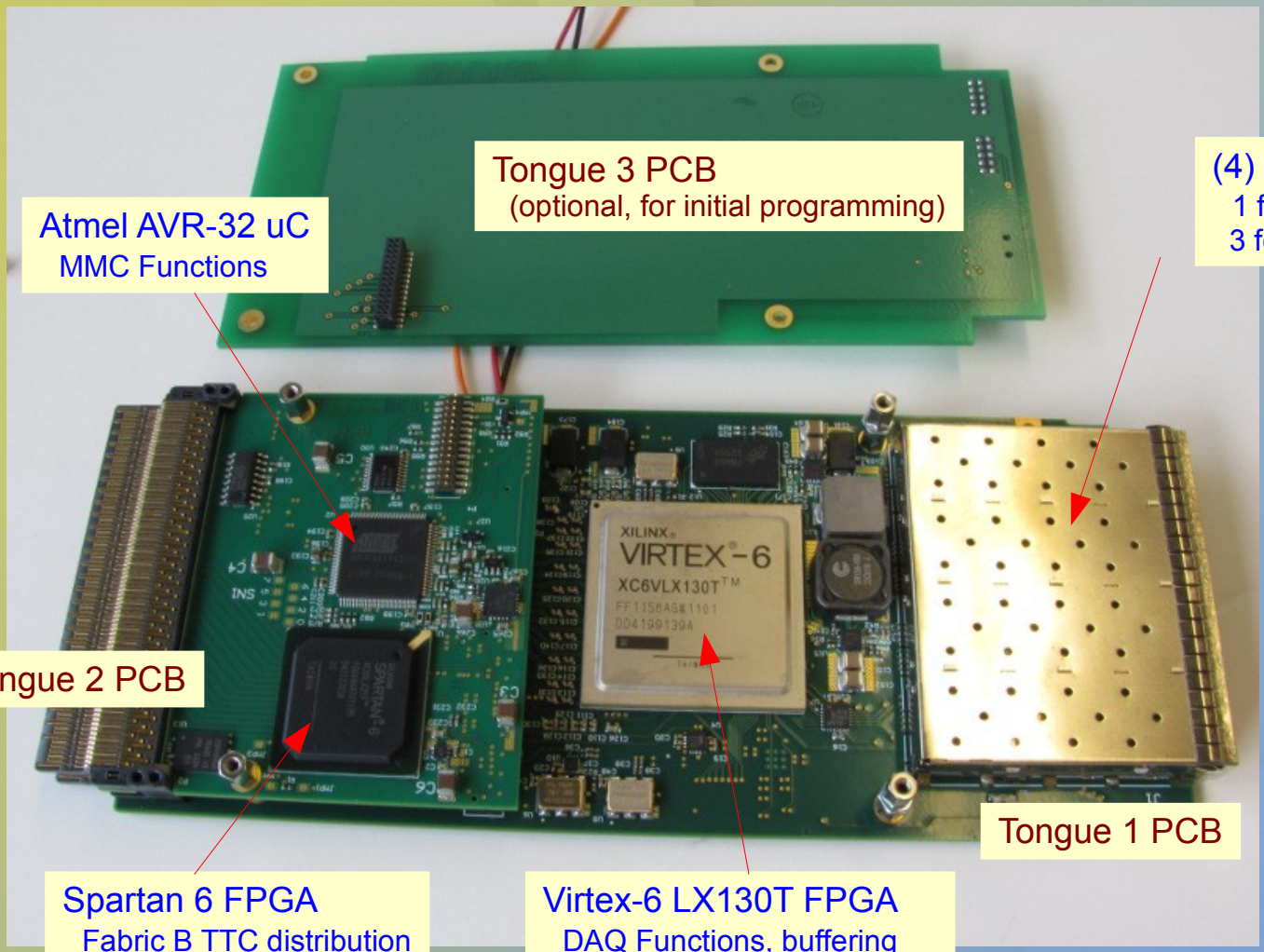


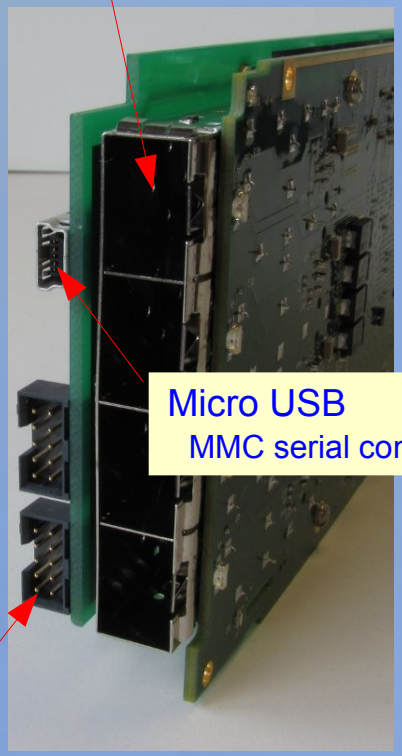
Quad SFP+
Cage

Connector to T3 provides:

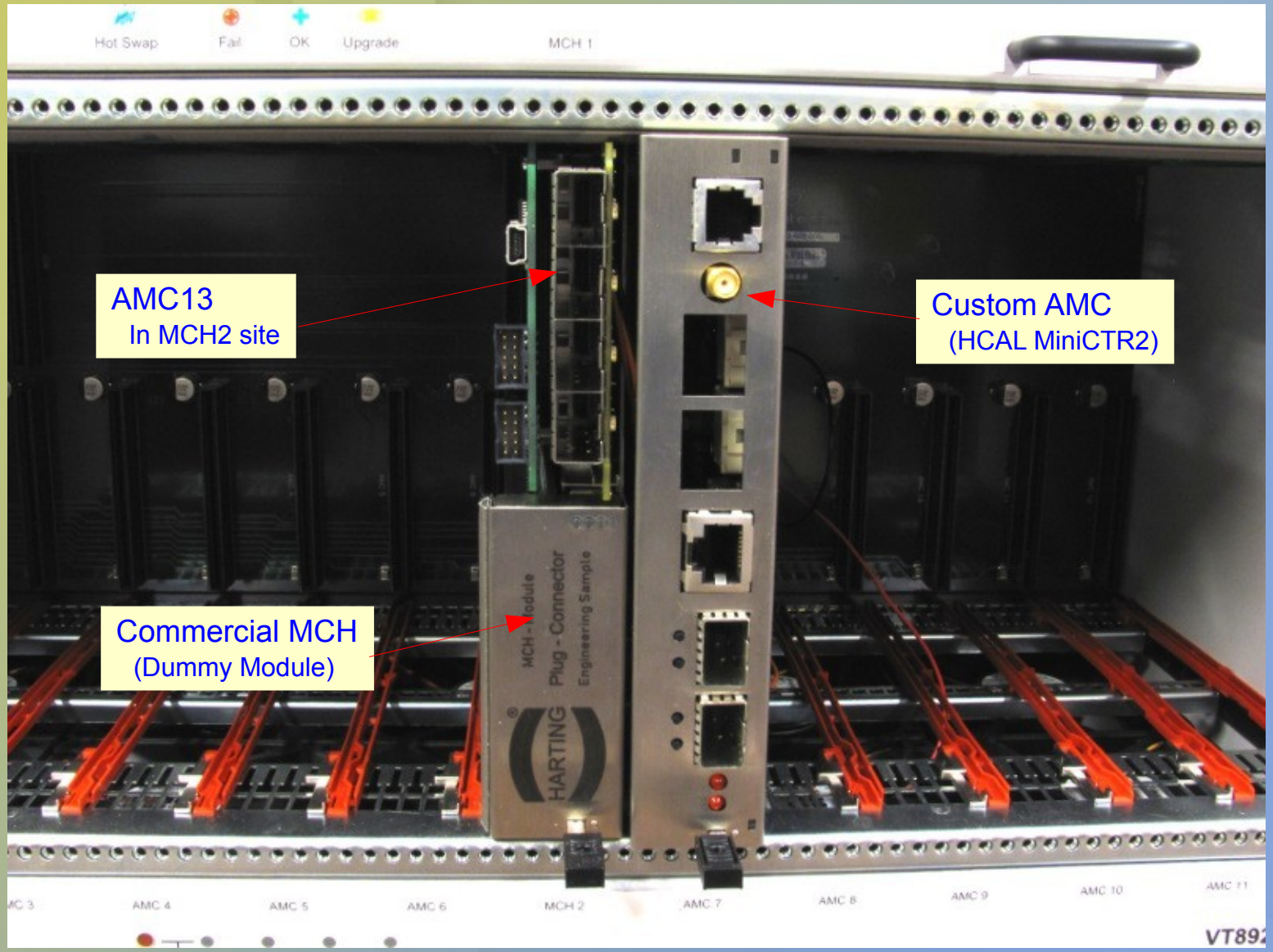
Power
JTAG (MMC and Xilinx)
Utility SPI
MMC serial console

AMC13 Hardware

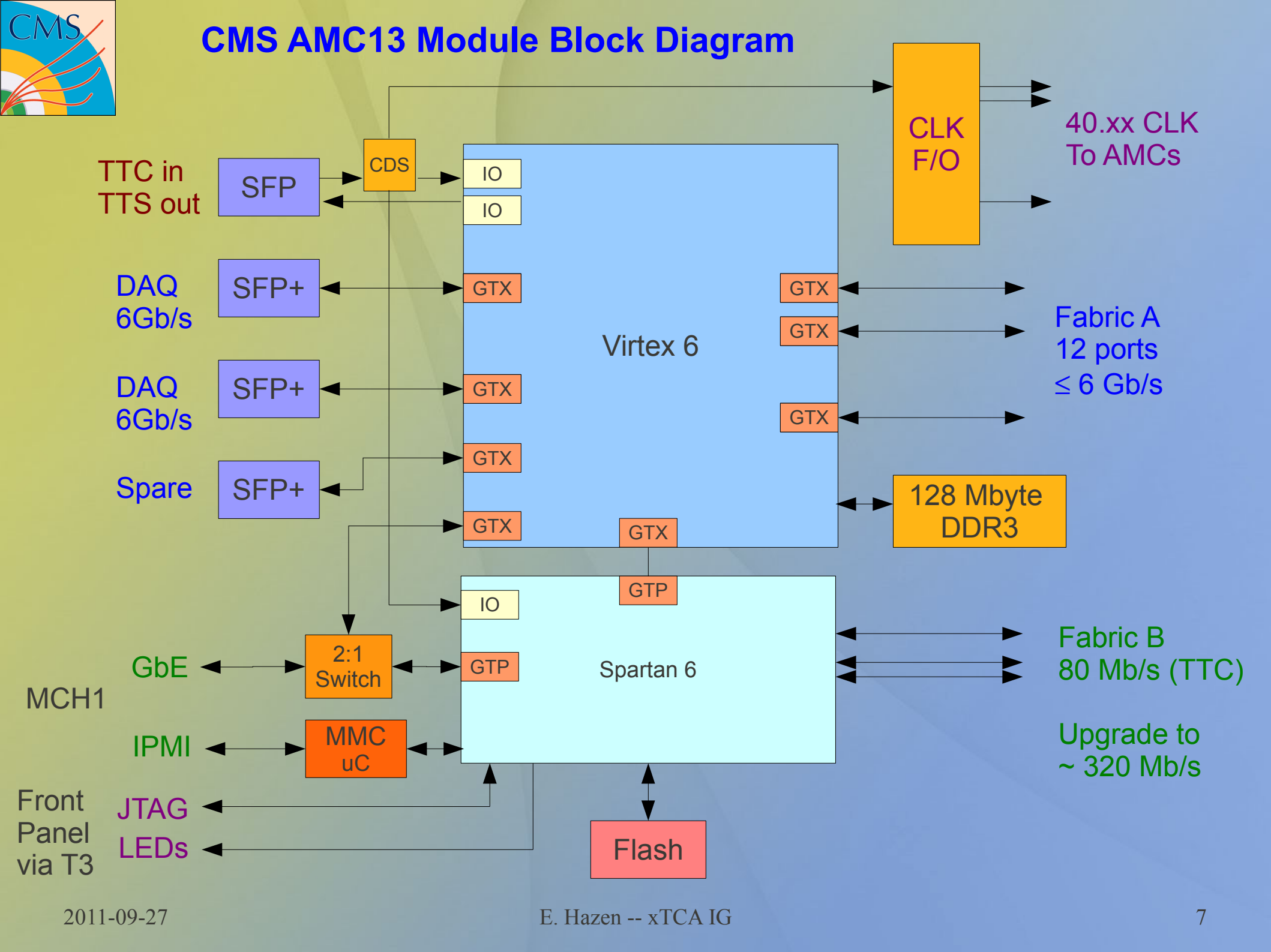




AMC13 in VT892 Crate



CMS AMC13 Module Block Diagram



uTCA Ports Use for CMS

Fabric	AMC Port	MCH	AMC13	Category	MCH Finger	CMS Use
A	0	Yes		Common Options	1	GbE
	1		Yes			DAQ
B	2	Yes			2	Spare
	3		Yes			Fast controls (TTC)
Clock	TCLKA	CLK1/2		Clocks		Spare
	FCLKA		CLK1/2			LHC Clock
D-G	4-7	Yes		Fat Pipes	3, 4	User
	8-11		Yes[2]			
H-K	12-15			Extended Fat Pipes		
	16-19					

Notes:

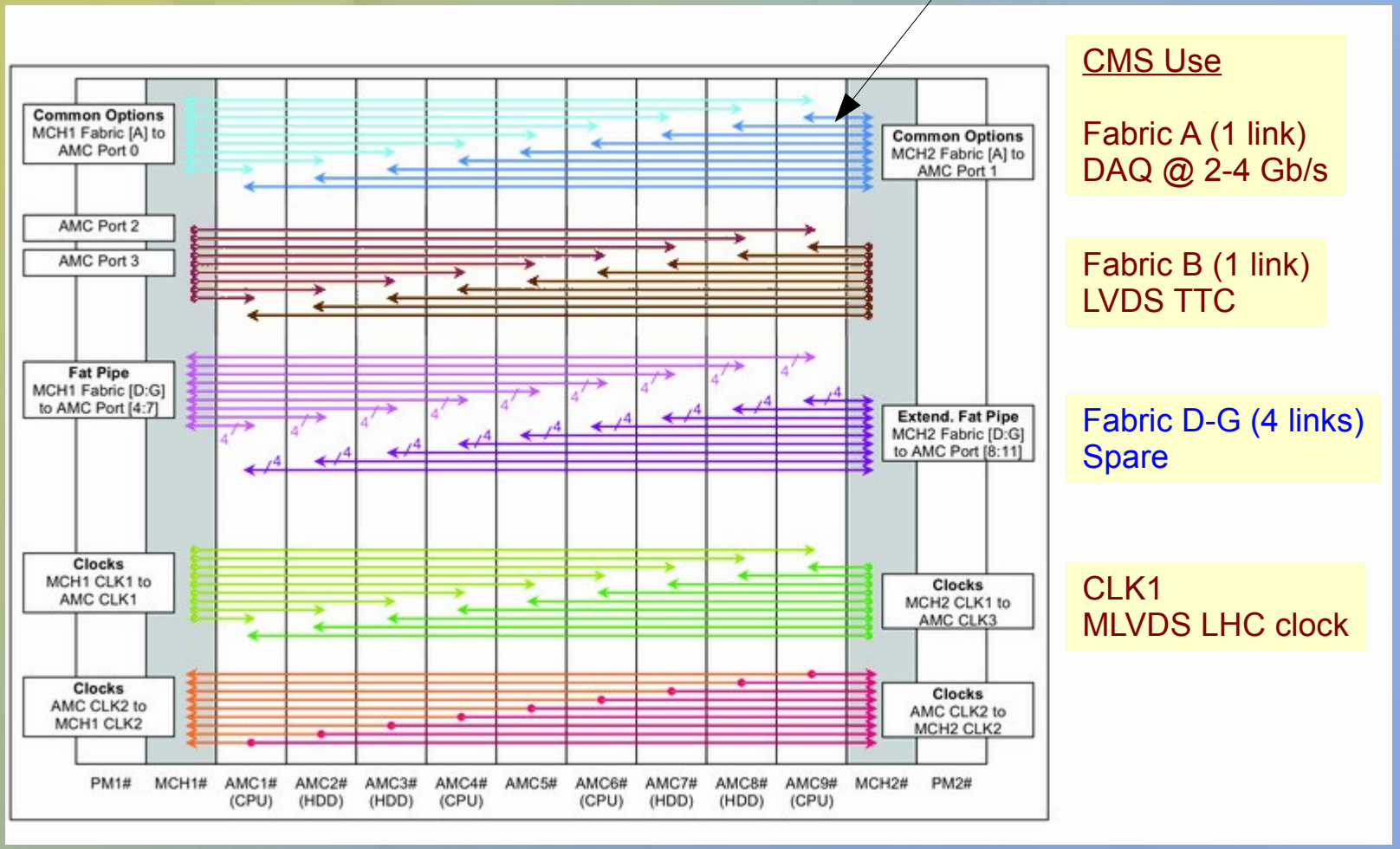
1. Port 1 (DAQ link) will be operated at a multiple of the 125 MHz GbE reference clock (2.5, 3.125, 5.0GB/s) in the AMC13 reference firmware. AMC designers are advised not to count on this... certain users may prefer to use the LHC clock as a reference for port 1.

2. "Fat pipes" fabrics D-G are routed to the T3/T4 connectors of the AMC13 but the standard AMC13 does not make any connection to these tongues. Users may implement their own boards. Contact me for details!

µTCA Dual-Star Backplane

Note: Interconnections can be customized by the backplane manufacturer inexpensively.

Bi-directional serial (up to 10Gb/sec) point-to-point links from each AMC to MCH (redundant links to each MCH)



Fabric A (1 link)
Gigabit Ethernet

Fabric B (1 link)
Spare

Fabric D-G
Spare

CLK1
Spare

CMS Use

Fabric A (1 link)
DAQ @ 2-4 Gb/s

Fabric B (1 link)
LVDS TTC

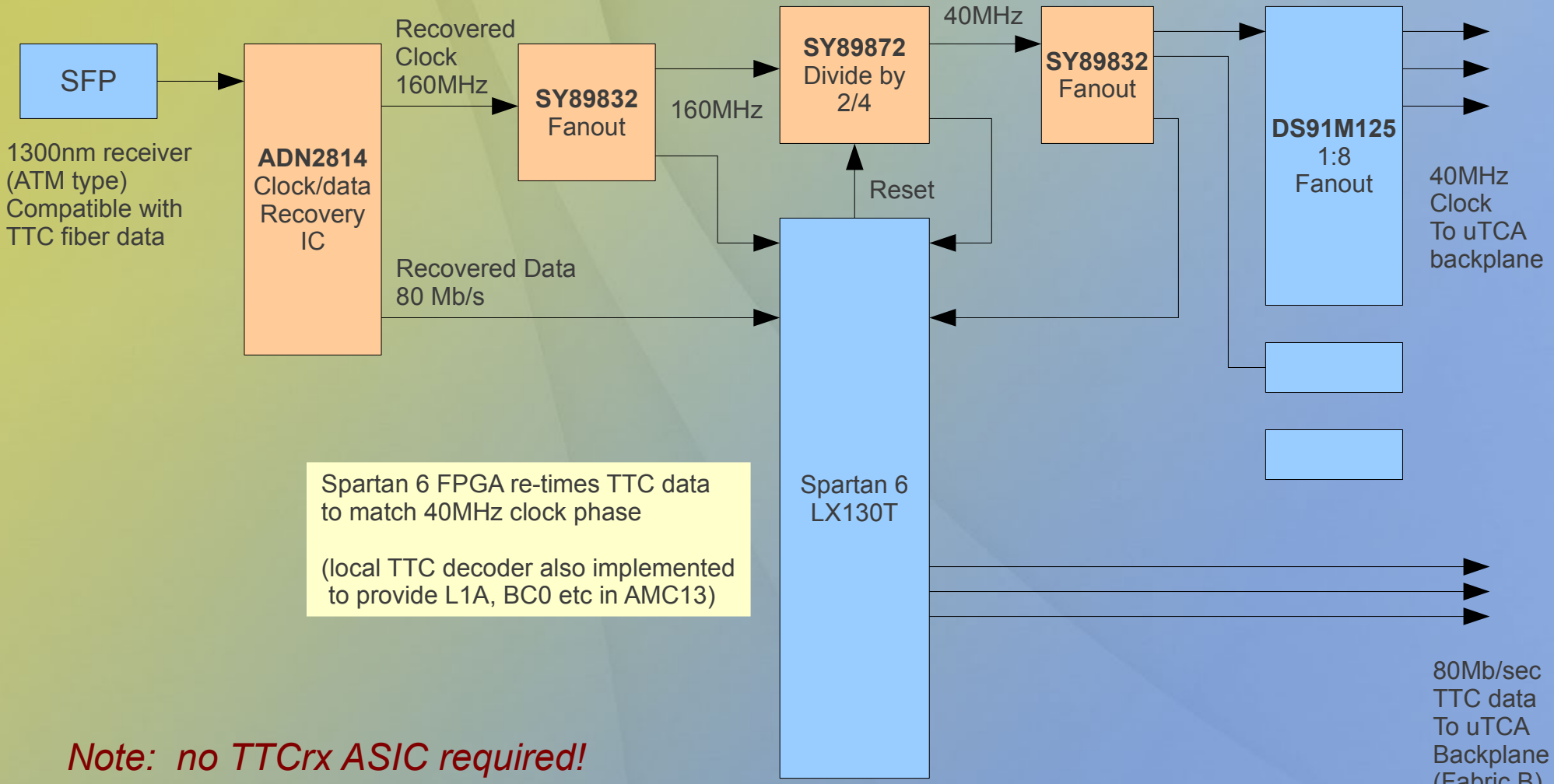
Fabric D-G (4 links)
Spare

CLK1
MLVDS LHC clock

MCH 1
Commercial /Std

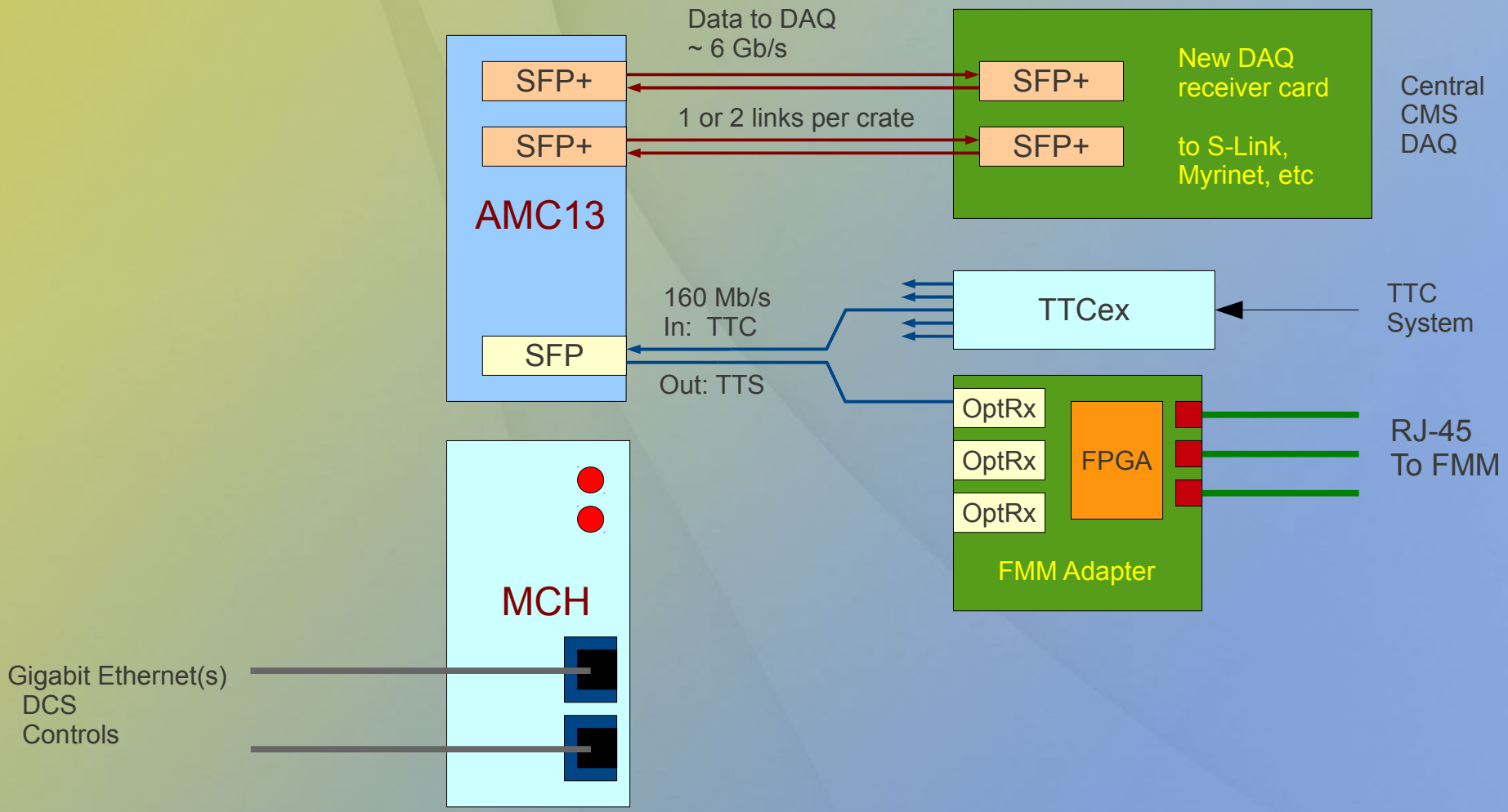
MCH 2 aka “AMC13”
Custom design for CMS

TTC / Clocks

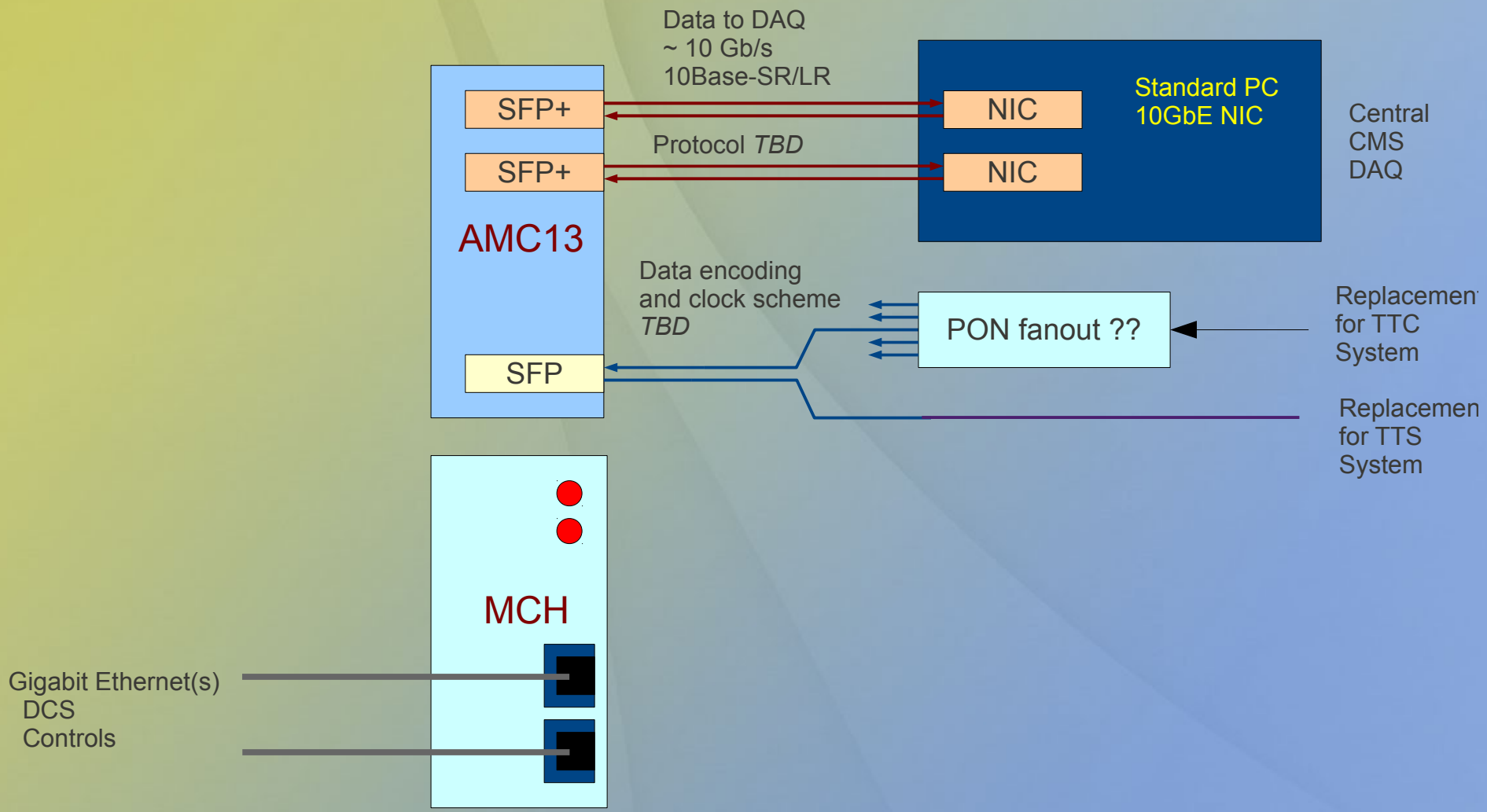


Note: no TTCrx ASIC required!

MicroTCA Interface to CMS
(Interim)



MicroTCA Interface to CMS
(Ultimate)



Status and Schedule

- 3 prototypes assembled and under test
- 8 more boards will be produced by end October 2011
- Initial Firmware development:
  - MMC (AMC standard plus useful extensions) by University of Wisconsin
  - Ethernet interface with IPBus / MicroHAL by Minnesota, Bristol, others
  - TTC / Clock distribution by Boston University
  - Flash programming via GbE
  - Prototype/demo DAQ for CMS HCAL
- First 3 items available by ~ Nov 2011

Highlights for Potential Users

- Documentation at http://www.amc13.info including draft crate/protocol definition document
- Backplane ports use and protocol (under) specification
  - If AMC designs comply with specifications, interface to i.e. CMS central systems is handled by AMC13
- MCH tongues 3, 4 available for users, i.e. for crosspoint switch.
  - Current no standard for T2/T3 connection :(so, commercial T3/T4 cannot be used.

Backup / Review Slides

Clocking Issue

- AMC13 provides LHC clock (40.xxx MHz) on MicroTCA CLK1.
- “Redundant Clock” Vadatech backplane routes this to AMC CLK3 (FCLKA).
- Some users have proposed to use commercial AMC which *requires* a 100MHz PCIe clock on this pin.
- This is incompatible with AMC13 clock scheme

DAQ Interface Upgrade

- We've invented a simple fiber-based demonstraton protocol for DAQ for AMC13 hardware testing (and possible HCAL TB use). This protocol can use two fibers per AMC13 (two HCAL FEDs).
- Tested extensively at 5Gb/s in lab using HCAL DTC board and Xilinx SP605 PCIe eval board
  - This board will be mounted in a PC with at least some software support (by us) for PCIe readout of DAQ data
- We are working with the CMS central DAQ group to develop interim and ultimate solutions for the DAQ link.