ATCA developments targeting ITER Fast Plant System Controllers

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FPSC will be used to diagnostics and Plant Systems in closed-control loops whose cycle times below 1 ms

Implemented in PCI family form factor and PCIe communication fabric running RHEL and EPICS

Standardized decisions on form factor, RT operating system and high performance networks

ADC capability
- e.g. number of channels, channel density, synchronization, resolution, sampling rate, filtering and galvanic isolation

Streaming of data to CODAC for visualization and archiving

Supervise other fast and/or slow controllers
FPSC | Hardware diagram

SDA
PCle x4 Cable
PCle x4 card DXH510
19" Industrial 4U PC
PCle host card HIB25x16H
PCle Cable X16
PCle host card HIB25x16T
ATCA shelf
Centellis AXP1440

SDN
PCle x4 Cable
PCle x4 card DXH510

TCN
Ethernet
IEEE-1588 card TSync-PCle-PTP

Sensors
Wiring
Input Signal conditioning

Actuators
Wiring
Output Signal conditioning

Signal Input

Data acquisition ATCA card
32 ch ADC / 8 ch DAC / 8 ch DIO

PCle
PCle
PCle
PCle
PCle
PCle
PCle
PCle
FPSC | Prototype

One Stop Sys. PCIe card & PCIe Cable

ATCA-CONTROLLER-PCle

Dolphin PCIe cable (DXH510)

Dolphin PCIe switch (DXS410)
For data archiving network

ATCA-MIMO-ISOL

Controller/PSH

Mini-CODAC

alpha version
MIMO Systems | high channel density & modularity

Another application:
ATCA based High-Speed Multi-Channel Data Acquisition Systems for W7-X
**Serviceability | RTM “Hot Swap”**

New module with RTM IO connectivity

Allowing hot-swappable use of RTM panel, for input-output
ATCA galvanic isolated digitizer node board
ATX-IO-Processor

- PICMG 3.0/3.4 and AXle compatible;
- 24/48 analog inputs, outputs or a combination of both;
- 24 digital inputs, outputs or a combination of both;
- RTM version with 16 fiber optics interfaces for remote actuators/sensors
- IPM controller module
Modular IO modules with galvanic isolation

Isolation Barrier (up to 1 kV)

Analogue sensor

Analogue actuator

Digital sensor / actuator
ATCA-IO-Processor
48 IO channels

ADC module
with ADC x2 and chopper mode

DAC module
with DAC x2
Signal Data Flow for acquired channels

Data transferred through 3 DMA channels
DMA Channel implementation allows changing output rate dynamically according to external events distributed through SDN.

**DMA #1**
Real-time data at programmable sampling rate

**DMA #2**
Data for archiving at programmable sampling frequencies

**DMA #3**
Data for continuous storage on the onboard memory

All data time-stamped before sent through DMA channel.
RT processing | MARTe RT framework being considered

- MARTe RT Framework
  - CAS
  - IOGAM

- FPSC-PSH IOC
  - PV db
  - AsynDriver
  - (configuration)

- Linux Device Driver
  - PCIe DMA#1 Continuous DA
  - PCIe DMA#2 Fast Event DA
  - PCIe PIO
  - PCIe DMA#0 (RT Flow)

- ATCA I/O
- FPSC-PSH DATA FLOW

- NetCDF Client
- MARTe

- MARTe RT Framework components
  - SDA
  - PON
  - SDN
MARTe is a collection of real-time threads scheduled by an internal state machine.

MARTe loads & links via communication protocol modules:
- State machine for operation (e.g. JET pulse sequence)
- I/O communications (e.g. CODAS or WEB interfacing)
- Additional (e.g. security or logger service)

Each real-time thread is totally configurable via configuration files.

Internal state machine:

Pool of driver and timing systems for complex applications (e.g. multiple threads with multiple sampling time).
EPICS not fast enough for FPSC
(for Hard-real-time)

See: A. Barbalace, et. al, Performance comparison of EPICS IOC and MARTe in a Hard Real-Time Control Application, in IEEE-NPSS RT 2010

MARTe is a solution to be considered and evaluated
Interface EPICS/MARTe implemented through Channel Access
High Performance computer

Several real-time algorithms will be tested e.g. FELIX, MW reflectometry profile reconstruction,…
1 kB, < 2 μs

SDN network
Reflective memory

Dolphin PCIe switch
DXS410

1 meter copper
0xad012210002

Node #4
Port #0

Adapter 0
Port #1

fpscpsb

1 meter copper
0xad012210015

Node #16
Port #10

SDA network
Supersockets

7x faster than ethernet

Switch 1
DXS410
0xad050209017

Switch 1
DXS410
0xad050209025

Node #8
Port #0

Adapter 0
Port #1

Node #12
Port #0

Adapter 0
Port #1

fpscpc

10 meters fibre
0xad012210009

10 meters fibre
0xad012210046

fpscminicodac
ATCA backplane synchronization | signals distribution

- Data time stamping using IRIG time distributed by hub card
  Internal time counter synchronised with IEEE-1588-2008 card
- Programmable timing unit for generating specific clock or trigger sequences for sampling
- Common synchronized clock
ATCA AMC Carrier / Hub
ATX-AMC4-PTP

ATCA cutaway quad-AMC module carrier

Compliance with ATCA extension for Physics ARTM (Advanced Rear Transmission Module - PICMG 3.8).

Most of mid/full-size COTS AMC modules can be installed

PCIe host x16

IEEE-1588
ATCA AMC Carrier / Hub
ATX-AMC4-PTP

PCIe on fabric
not available from industry

RTM connectivity

Support multiple processors on AMC slots or external through PCIe cable connection

FPGA for timing & synchronization
IEEE-1588 to IRIG on backplane + 100 MHz clock

IPM controller module
ATCA AMC Carrier / Hub
ATX-AMC4-PTP

PCle on fabric
not available from industry

RTM connectivity

Support multiple processors on AMC slots or external through PCIe cable connection

FPGA for timing & synchronization
IEEE-1588 to IRIG on backplane + 1 MHz clock

IPM controller module
Timing signals are managed and routed by a crosspoint-switch implemented on a Virtex-6 FPGA

Each clock signal source may be independently located
(on each of the AMC cards, RTM or ATCA backplane)
Timing | White Rabbit based

@ CERN

(i) Enabling the compatibility with IEEE-1588-2008 and
(ii) Porting WR PTP core to Spartan-6 and Virtex-6 FPGA.

Both goals are in sync with FPSC, which requires an IEEE-1588-2008 core implemented on a Virtex-6 FPGA.

Additionally,

WR compatible interface will add sub-nanosecond timing compatibility, which may be of interest to ITER in case specific more demanding timing applications arise in the future.

@ IPFN

(i) Porting current version of WR PTP core and associated software to specific hardware resources of ATCA-AMC-CARRIER board;
(ii) Testing WR PTP core in compatibility mode and measure jitter of PPS signals (goal: ~50 ns RMS);
(iii) Testing WR PTP core in WR mode with a WR switch and measure jitter of PPS signals (goal: ~100 ps RMS);
FPSC | ITER Prototype

ATCA shelf

Controller/PSH

Mini-CODAC & archiving

HPC

beta version

PCIe

SDA

Gb Ethernet

PON

TCN

SDN

PCIe
EPICS interface at Mini-CODAC

Hardware Monitoring & Settings

High Performance Networks Monitoring

System State Machines

Control & Data Acquisition
Contributing to ITER standardisation effort with ATCA solutions!

- **MIMO system** | high channel density
- **Modular / Expandable**
- **Galvanic Isolated** | 1 kV
- **Serviceable** | Remote hardware management, modularity, RTM IO
- Change of output rate dynamically according to external events
- **Real-time complex algorithms** | MARTe
- **Redundancy and high availability**
- **Timing and Event management**
- **Integration into ITER CODAC** | EPICS, HMI, PSH
- **COTS available** | ?

Thank you!