Microfluidic Cooling for Detector and Electronic

A. Mapelli & P. Petagna
CERN PH-DT

Reporting on behalf of
D. Bouit, J. Daguin, L. Kottelat, A. Mapelli, J. Noel, P. Petagna – CERN PH-DT
K. Howell – Georges Mason University / CERN PH-UFT
G. Nuessle – Universite Catholique de Louvain / CERN PH-UFT
A. Pezous - CSEM
P. Renaud – EPFL-LMIS4

OUTLINE:
Motivations for micro-channel cooling in HEP
Micro-technologies involved
First possible HEP cases: the NA62 GTK
the ALICE ITS upgrade
the LHCb VELO upgrade
Other ongoing R&D programmes on micro-channel cooling
Conclusions and perspectives
Motivations I : starting point

**Twepp 2009 (Paris):** J.R. Thome, J.A. Olivier, J.E. Park  *Two-Phase Cooling of Targets and Electronics for Particle Physics Experiments*

- Main focus: high power densities, up to as high as 350 W/cm$^2$;
- However, interesting preliminary features also for HEP applications;
- State-of-the-art heat transfer and pressure drop models presented;

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**Geometry sensitivity for liquid cooling**

**Liquid vs. evaporative**

**Channel parameters used for Thome’s preliminary simulations based on the NA62 GTK test case**

**Silicon µ-channel cooling device used for testing at EPFL**

**Typical laboratory fluid distribution!**
Motivations – II: advantages for HEP

- MINIMIZATION OF MATERIAL BUDGET
  - ultra thin Si cooling plates and tiny (PEEK?) pipes
  - no mechanical components required for thermal bridges

- COOLING POWER ENHANCEMENT
  - very high heat transfer coefficients (very small Dh)
  - very high heat flux (large S)

- REDUCTION OF $\Delta T$ BETWEEN HEAT SOURCE & HEAT SINK
  - large surface available for the heat exchange (cold plate vs. cold pipe)
  - natural minimization of the thermal resistance between the source and the sink

\[ Q = hS(T_w - T_f) \]
Motivations – III: thermal performance

Examples of cooling solutions in LHC trackers

Lower temperatures are envisaged for the future Si-trackers at SHLC. This has non-negligible technical impacts on the cooling plants.

With a standard cooling approach, the $\Delta T$ between the module and the fluid ranges between 12 and 20 °C (small contact surface + long chain of thermal resistances).

$\Delta T \sim 15$ °C

Pix

Strip

Substrate

Heat sink

$\Delta T \sim 10$ °C

ATLAS IBL staves

$\Delta T \sim 10$ °C

ATLAS IBL staves

$\Delta T \sim 5$ °C

$\Delta T \sim 5$ °C

ATLAS IBL staves

Carbon foam + CFRP skin

Cooling pipe

Adhesive

Si sensor

Si chips

Si cold plate

NO CTE DIFFERENCE!
Motivations – IV : impact on material budget

Present LHC large Si trackers (ATLAS and CMS) ~ 2% $X_0$ per layer

SLHC “phase II” upgrade: “significant” reduction needed

Future trackers at ILC ~ 0.1 ÷ 0.2% $X_0$ per layer
Microfabrication technologies are derived from microelectronics to fabricate microsystems and microfluidic devices.

Bulk micromachining: mechanical structures are etched in the wafer.

Surface micromachining: layers of material are deposited on the wafer and structured.

Commonly used substrates and materials include Silicon, SOI, Glass, Pyrex, Quartz, Polymers (SU-8, Polyimide, Parylene), Metals,...

Fully laminar flow ensures high degree of predictability and control. No sources of instabilities and/or vibrations.
Micro Fabrication: Etching

Etching of microchannels

Dry Etching
Plasma, RIE, DRIE

Wet Etching
Chemical: KOH, TAMH, PGMEA

Silicon DRIE
Anisotropic, vertical walls

Silicon KOH
Walls depend on crystal orientation

SU-8 photoresist
Vertical walls
Micro Fabrication: Bonding

Anodic Bonding
- Pyrex-Si, Si-Pyrex-Si
- Temp. ~400°C
- Voltage 50 ÷ 1200 V
- Tool pressure

Direct Bonding
- Silicon Fusion Bonding
  - Si-Si, Si-SiO₂
  - Annealing ~1000°C
  - Optional tool pressure
- Plasma-activated
  - Low temp.

Required:
- wafer flatness
- Surface roughness < 1 nm

Intermediate layer bonding
- Polymers (SU-8, Parylene, ...)
- Thermocompression
  - Eutectic (AuIn, AuSn, AuSi, AlGe..)
- Glass Frit

Bond Example
Good bond: edge with concave shape
Poor bond: edge with rough convex shape
Micro Fabrication: Thinning

**Wafer thinning**
- Grinding
- Chemical Mechanical Polishing
- Etching

**Local thinning**
- Etching (dry or wet)
NA62 GTK – Requirements and Basic Concept

μ-channel cooling plate

Final target: 0.10 – 0.15 % $X_0$
(Silicon thickness < 150 μm)

• Priority: minimize $X_0$
• Acceptable DT over sensing area ~ 5 °C
• Dimension of sensing area: ~ 60 x 40 mm
• Max heat dissipation: ~ 2 W/cm²
• Target T on Si sensor ~ -10 °C

“Keep it simple at first” approach:

liquid C$_6$F$_{14}$ cooling

Design optimization

Pressure drop for different manifold depths

3 INDEPENDENT STATIONS: “SIMPLE” SYSTEM
NA62 GTK – Details of μ-channel Design

Manifolds 280 µm deep
Max width = 1.6 mm

Through holes

Wall thickness between channels: 200µm (for Si fusion bonding) or 50mm (for Si-Si anodic bonding)

Channels: 100 ÷ 300 µm wide
100 ÷ 70 µm deep

NA62 baseline design holds ~ 20 bars.
Critical point at the level of the manifold’s maximum width (1.6 mm).
Safety factor: 3 to 5
NA62 GTK –μ-channel Thermal Performance

4g/s, Inlet -16.8C, No Power

4g/s, Inlet -16.8C, Digital 5.4W, Analog 14.1W

Max ΔT on sensor ~ 6 °C

Fluid-sensor ΔT ~ 6 °C

Connectors

Wafer equipped with GTK simulator

Outlet

Heater 1

Heater 2

Heater 3

Inlet
NA62 GTK – Second Order Optimization

Dual inlet / dual outlet design allows for more uniform flow distribution and for sensible pressure drop reduction.

**Influence of channel geometry on total pressure drop**

Perfluorohexane with dual system @-25°C with 9.84 g/s for 48 Watts | 200 micron walls

<table>
<thead>
<tr>
<th>Channel width [µm]</th>
<th>No. Of Channel</th>
<th>Channel Depth</th>
<th>Pressure Drop [kPa]</th>
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<tr>
<td>466.67</td>
<td>45</td>
<td>6.39</td>
<td>4.76</td>
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<tr>
<td>400.00</td>
<td>50</td>
<td>6.69</td>
<td>4.96</td>
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<td>345.45</td>
<td>55</td>
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<td>300.00</td>
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<td>7.42</td>
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<td>261.53</td>
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<tr>
<td>100.00</td>
<td>100</td>
<td>15.84</td>
<td>11.55</td>
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</table>

A second round of CFD and structural parametric analysis brings to a fully compliant solution: now submitted to the collaboration for approval.

Drawing not to scale
All dimensions in µm
ALICE ITS – First Approach

Stave from SPD to ITS

Conventional configuration

Micro-channel cooling approach

Support Structure | Material budget X/X0 (%)
--- | ---
Carbon foam structure | 0.22 – 0.34
Polyimide micro-channel structure | 0.085 – 0.13
Silicon micro-channel structure | 0.07 – 0.11

Two working possibilities:
• evaporative C4F10
• monophase water in underpressure
ALICE ITS – Sideline Micro Channels?

Remove silicon cooling plate where not needed.
ALICE ITS – Open Issues

Long stave (~ 200 mm):
• multi-module $\mu$-channel solution? (multi connector or module-to-module junction)
• Single $\mu$-channel from 12” wafer? (higher cost and more difficult handling of thinned devices)

“Packed” barrel configuration”
• Need for a reliable in-plane $\mu$-connector. Discussions ongoing with CSEM for a common R&D programme
LHCb VELO – First Approach

Power dissipated: \(~2\) W/cm\(^2\)
Cooling: evaporative CO\(_2\)
Cooling substrate in acceptance: 250 ÷ 500 µm
go out of acceptance: \(~1\) mm

Out of acceptance up to 1 mm Si!

CO\(_2\) saturation pressure at room temperature: high pressure is not an issue!
Small issue:
Out-of-plane connector is acceptable, but a special reduced size production must be requested (Nanoport connectors rated up to 103 bar!)

Big issue:
LHCb VELO is inside the secondary LHC vacuum: absolute reliability is required!!! Main problem: QA/QC of the hermetic bond between the two wafers
"The CMOSAIC project is a genuine opportunity to contribute to the realization of arguably the most complicated system that mankind has ever assembled: a 3D stack of computer chips with a functionality per unit volume that nearly parallels the functional density of a human brain. CMOSAIC's aggressive goal is to provide the necessarily 3D integrated cooling system that is the key to compressing almost 10^12 nanometer sized functional units (1 Tera) into one cubic centimeter with a 10 to 100 fold higher connectivity than otherwise possible"
Other R&D Programmes – Polyimide μ-channels

Polyimide MicroChannel cooling
R&D for ALICE-ITS upgrade

Polyimide based micro-channel heat sink represents an interesting possibility to cool down the pixel stave using single phase cooling.

Axonometric view of Micro channel cooling

Cross section of one SPD layer

Material budget evaluation

Cooling structure assembly materials
- Pyralux® PC 1020 (polyimide) 200μm
- Pyralux® LF7001 (Kapton®) 24μm
- Pyralux® LF110 (Kapton®) 50μm

<table>
<thead>
<tr>
<th>Material</th>
<th>Radiation length [cm]</th>
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<tbody>
<tr>
<td>Kapton</td>
<td>28.6</td>
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<tr>
<td>H₂O</td>
<td>36.1</td>
</tr>
</tbody>
</table>

Courtesy of I. Sgura and C. Pastore (INFN Bari)
Other R&D Programmes – Polyimide μ-channels

CFD analysis results
R&D for ALICE-ITS upgrade

CFD simulations have been carried out using a commercial CFD software package, Fluent 6.0

Assuming Water in Single Phase

Single channel temperature distributions

T_{water\ IN} 15°C

Top layer

T_{water\ OUT} 18°C

Axonometric view single channel

Inlet section channel

Middle section channel

Outlet section channel

L = 20 cm
W = 1.6 cm
q = 0.5 W/cm²

16 channels 800 x 200 μm²

IN

OUT

Courtesy of I. Sgura and C. Pastore (INFN Bari)
Other R&D Programmes – Polyimide μ-channels

Prototype production and test
R&D for ALICE-ITS upgrade

I Prototype

The first prototypes have been fabricated (R. De Oliveira, CERN TM-MPE-EM) with successful for the experimental tests.

16 channels 800 x 200 μm²

Top view

Local micrograph

The 3D reconstructed roughness on 50 x 50 μm² surface

Experimental test

Leak and water compatibility

Support-distributing frame

Micro channels

Part of the set up for the ongoing mechanical and thermo-fluid dynamic tests

Courtesy of I. Sgura and C. Pastore (INFN Bari)
Conclusions

Micro-channel cooling features highly interesting potentialities for HEP applications

Available $\mu$-technologies allow for a palette of solutions adapted to different requirements and specific environments

A working solution for the **NA62 GTK** is ready for submission to the experiment

Activities for the **ALICE ITS** and for the **LHCb VELO** upgrades have started

Parallel activities are ongoing outside CERN for hi-power computing (IBM, EPFL, ETHZ) and for HEP (Bari/CERN Polyimide $\mu$-channels for ALICE ITS)

$\mu$-channel cooling is perfectly suited for future **3D architectures** (if any...)

**Main issues to be addressed:**
1) Reliable QA/QC process for hermetically sealed channels (bonding)
2) Reliable miniaturized in-plane connections
**PHASE I**: μ-channel cooling plates conceived to adapt to an existing electronics design and placed in good thermal contact (NA62 GTK)

**PHASE II**: μ-channel cooling plates conceived in connection with the electronics design and integrated at the same time in the module’s architecture (maybe already possible with ALICE and LHCb phase I upgrades)

**PHASE III**: μ-channel cooling integrated in the module conception:
- a) In the sensor? Compatible with physics performance?
- b) In the chips? When? By whom?
- c) In the Si-Interposer? (should 3D become real...)