

DEPARTMENT OF
INFORMATION
ENGINEERING
UNIVERSITY OF PADOVA



DC/DC CONVERTER FUTURE PLANS

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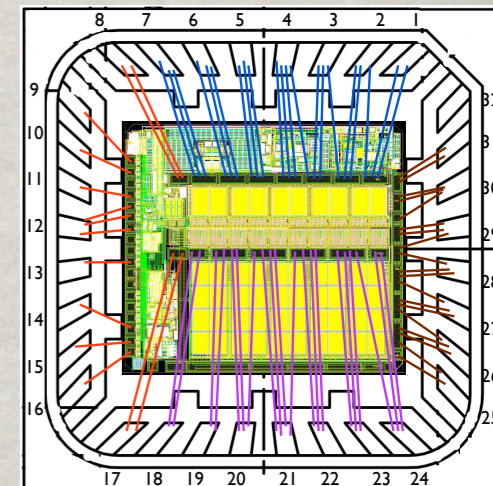
Twepp 2011, Vienna 26-30 September 2011

ASIC DESIGN

	AMIS2	IHP1	IHP2	AMIS4
Full control loop	✓	✓	✓	✓
Dead times' handling	Fixed	Adaptive (QSW)	Adaptive (QSW and CCM, sharp transition)	Adaptive (QSW and CCM, smooth transition)
On-chip regulator(s)	No	No	✓	✓
Soft Start	Simple RC	Simple RC with comparators	Full sequence with comparators	State machine
Over-I protection	No	No	✓	✓
Over-T protection	No	No	No	✓
Under-V disable	No	No	No	✓

↕
Used in system tests

↕
Taped-out Jan2011
still under tests,
preliminary results



AMIS4: FUTURE PLANS

Work to be done in AMIS4

A compact and optimized board has been design by Georges (in these days under tests, results soon available) + Focused Ion Beam will be used to modify some connection.

Irradiation test under heavy ions and protons are foreseen in fall 2011

Definition of the bond-diagram for user applications (next weeks)


packaging (Europractice, ASE?) for user applications (fall 2011)

ASIC DESIGN

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ASIC DESIGN

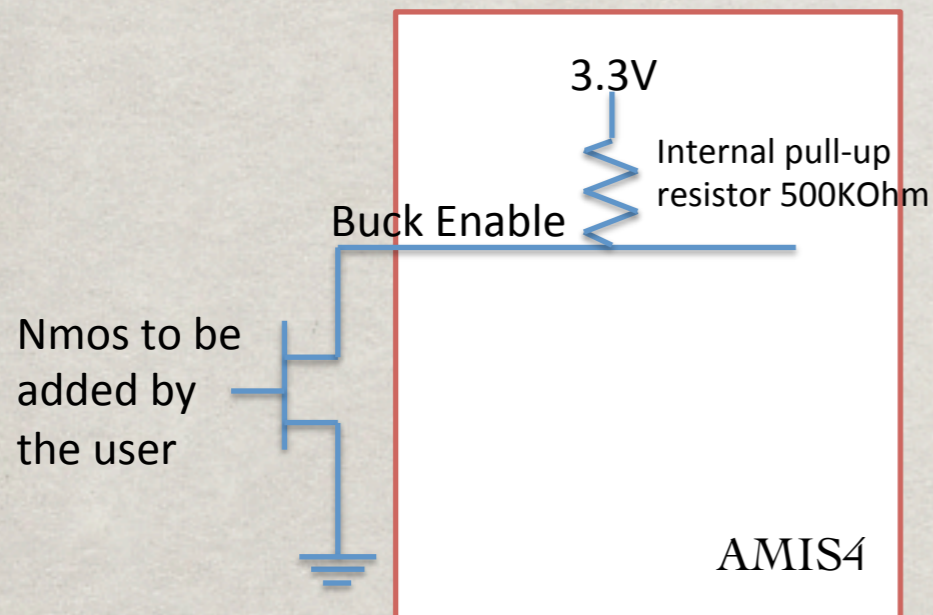
	AMIS2	IHP1	IHP2	AMIS4	AMIS5
Full control loop	✓	✓	✓	✓	✓
Dead times' handling	Fixed	Adaptive (QSW)	Adaptive (QSW and CCM, sharp transition)	Adaptive (QSW and CCM, smooth transition)	Adaptive (QSW and CCM, smooth transition)
On-chip regulator(s)	No	No	✓	✓	✓
Soft Start	Simple RC	Simple RC with comparators	Full sequence with comparators	State machine	State machine
Over-I protection	No	No	✓	✓	✓
Over-T protection	No	No	No	✓	✓
Under-V disable	No	No	No	✓	✓



as AMIS4
 + small modification for fixing the AMIS4 issues
 + change for System Compatibility (open drain for power good and pull-down for enable)

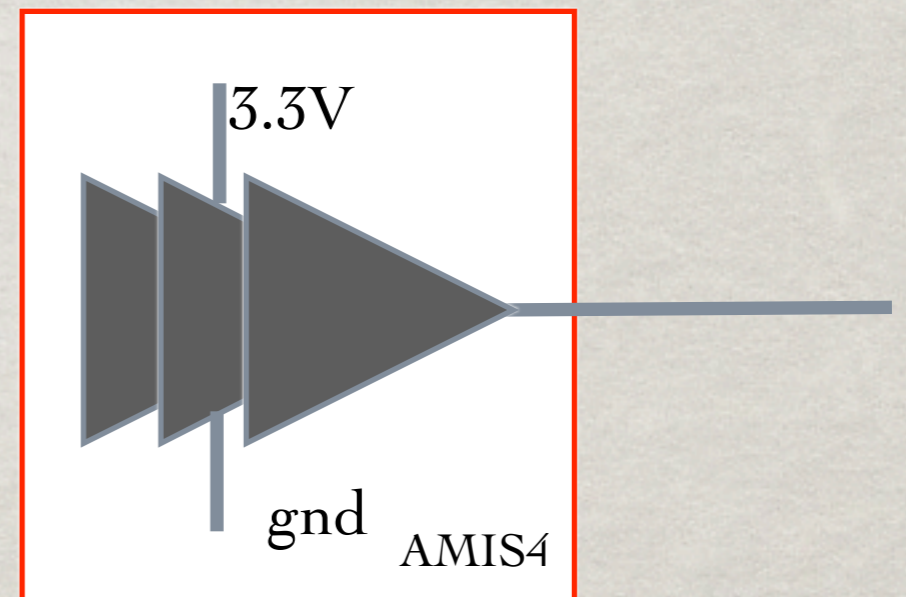
BUCK ENABLE AND POWER GOOD IN AMIS4

Buck Enable



pull-down
configuration

Power Good



Power Good is

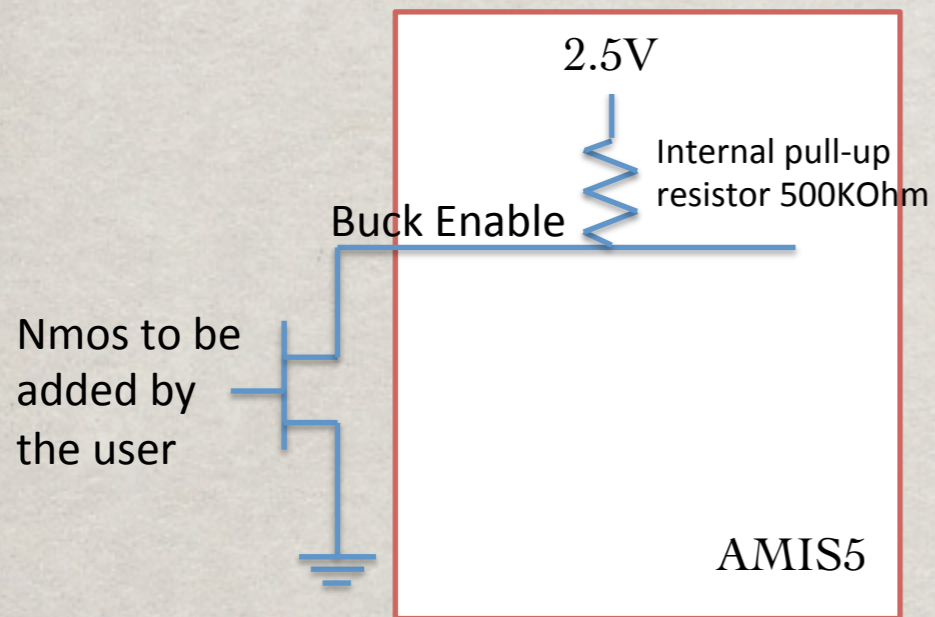
3.3V if the converter works without problems

0V during the soft start and when a fault from the protection circuits is detected:

- OverCurrent,
- OverTemperature
- input UnderVoltage

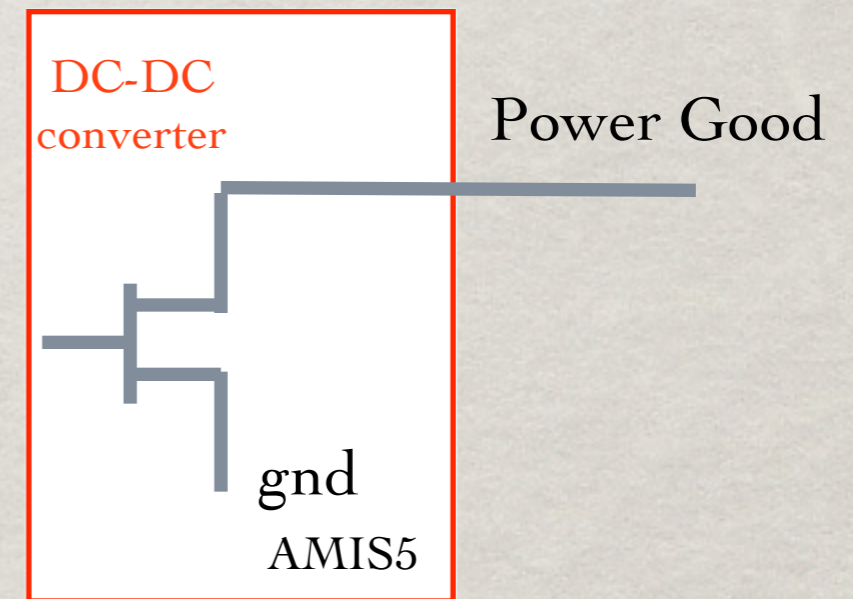
NEW SIGNALS IN FUTURE ASIC

Buck Enable



pull-down configuration

Power Good



open drain configuration

PLAN FOR AMIS5

Design of AMIS (fall 2011)

Submission (January 2012)

Chip back in June-July 2012



ASIC DESIGN BACKUP TECHNOLOGY

We are investigating a backup technology :

0.18um High Voltage technology with transistors that can stand 20V.

Preliminary TID and Proton radiation tests gave good results

A test chip has been submitted in July

Radiation (in particular heavy ions) tests will be done during fall 2011

CONCLUSIONS

