Switched Capacitor DC-DC in FE-I4

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FE-I4 Introduction

- Designed in a 130nm feature size bulk silicon process.
  - Chip size: 2cm × 1.9cm
  - Pixel array: 80col × 336row (26,880 pixels)
  - Pixel size: 250um × 50um
  - For each pixel: free running CSA + shaping + discriminator
  - Sophisticated digital logic processing "firing time" and "time over threshold (TOT)" of each pixel, and transmitting data out of the chip via a pair of 160Mb/s differential signals.

- Will be used for IBL upgrade and future
Power Options for FE-I4

- Basically the power rail inside FE-I4 are divided into 4 groups and attached to separate pads:
  - VDDD1/GNGD1, VDDD2/GNDD2, VDDA1/GNDA1, VDDA2/GNDA2
  - In addition dedicated power nets for PLL, EFUSE and T3 isolation as well.
- 3 isolated power modules in the chip.
  - Two linear-shunt LDOs (ShuLDO) -> Laura's talk.
  - One switched capacitor DC-DC converter -> this talk.
  - Neither is hard-wired inside the chip. Thus Wire connections outside the chip needed.
Power Modules in FE-I4 Layout

Pixels

FE-I4A Layout

DC-DC & ShuLDO1

Magnification of DC-DC & ShuLDO1

ShuLDO2

250um pads for power modules while 100um pads for signals

DCDC_IN
Cpump1
Cpump2
REG1_IN
REG1_OUT
REG_GND
DC-DC configuration in FE-I4

- CLOLK is provided from outside the chip. This clock also serves as auxiliary clock for the chip.
- Ceramic capacitors used for the test. Cpump is mounted on the board as close to the chip as possible.
- DCDC_OUT and ShuLDO1_IN are connected in the chip and share the same pad.
- As a "divide-by-two" converter, ideally: Iout=2Iin & Vout=Vin/2.
DC-DC Circuit in FEI-4

- **Non-overlapping Clock generator:**
  - generates 3 internal clock signals from CLK_IN
  - the same frequency but different phase.

- **Charge pump:**
  - consists of 4 transistors working as switches
  - manipulates the pump capacitor under control of clock signals.
Non-overlapping clocks

- 5ns gap between CLK_BOT1 and CLK_BOT2 to eliminate adverse discharging.

During transition, need these gaps to guarantee correct sequence of switching.

Not to scale

No Good!
Avoid it!

Charge Phase

Discharge Phase

Adverse discharging
Testing Results
Efficiency vs Clock frequency

Vin=3.3V, Rload=5Ω

- Simulation result shows Vefficiency around 90%, while the test result shows Vefficiency of about 84% (Schematic simulation).
  - Not bad.
  - Post-layout simulation probably will give us different numbers.
- 1MHz is the optimal frequency for this tested chip.
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Rout on irradiated chips

- 3 chips irradiated in Los Alamos last Dec. with different dose.
  - We made new tiny boards to test them (talk about it later).
- The chips seem immune to irradiation.
- 3.3V thick oxide transistors were used in the DC-DC design, while in commercial chips this kind of transistors are normally used in I/O circuit. This is the first measurement showing their radiation-hardness property.
This problem remains unsolved so far.
DC-DC induced noise

Measured on this board!
We have different setup improved the noise.
(next slide)

- Noise increased as long as DC-DC running even without using it to power the chip.
- Noise depends on DC-DC current.
- To investigate this problem, we made some changes to the DC-DC external configuration shown on next page.
To test DC-DC in different external configuration

- We made some tiny boards, which sit on top of the chip and wire bonded to it.
  - the capacitors needed to operate DC-DC located on the tiny boards.
  - external connection by wires attached to them.
- By this way, we separated DC-DC operation from the big board.
  - and made tests on irradiated chips possible.
Noise map when using tiny boards

- The noise increased only slightly.
- It proved that the noise in the previous measurement came from outside rather than inside of the chip.
  - If the noise is internal, there's no way to get rid of it by external configuration.

**Normal Power**

**Powered by DC-DC**

unstable pixels, safe to ignore them
Conclusion

• Current DC-DC design in FEI-4 seems good enough to power even analog part of the chip. Promising!
• 3.3V thick oxide I/O transistors showed their radiation-hardness property.
• More efforts on the external configuration needed if one wants to put it into real use.
• Post-layout simulation needed to understand the discrepancy between measurement and simulation, in terms of efficiency and ripple voltage.
Future

• The DC-DC circuit will remain in the production version of FEI-4(FEI-4B) but IBL won't use it for lack of time to fully understand and refine it.

• More complex DC-DC circuit might be introduced into the chip as following-up of current efforts.
• Thanks for paying attention!
Backup Slides
Charge pump core schematic

PFET:
Ron~1.75Ω

NFET:
Ron~0.45Ω
Running DC-DC standalone

- Running DC-DC but not using it to power the chip (the DC-DC converter is not hard-wired inside the chip).