The ATLAS IBL BOC

N. Schroer[1], G. Bruni[2], J. Joseph[3], N. Krieger[4], A. Kugel[1], P. Morettini[5], M. Neumann[6], A. Polini[2], M. Rizzi[2], R. Travaglini[2], S. Zannoli[2], A. Zoccoli[2], M. Bruschi[2], I. Dantone[2], D. Falchieri[2], J. Dopke[7], T. Flick[6], A. Gabrielli[2], J. Grosse-Knetter[4], T. Heim[6]

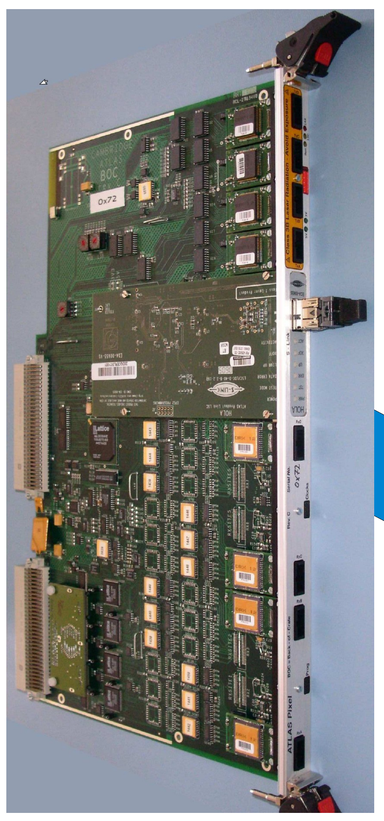
[1]ZITI-University of Heidelberg, [2]University & INFN Bologna, [3]LNBL Berkeley, [4]University of Goettingen, [5]INFN Genova, [6]University of Wuppertal, [7]CERN

Motivation

In 2013 an additional layer, the **Insertable B-Layer (IBL)** will be added to the pixel detector of the ATLAS experiment at the LHC at CERN. For this fourth and innermost layer 448 newly developed pixel sensor chips (FE-I4) are used which will provide about 12 million pixel. For the readout of the IBL new off-detector electronics are needed as the FE-I4s feature an increased readout bandwidth which can not be handled by the current system. To provide a degree of backward compatibility the new system will keep the structure of VME card pairs: The **back of crate card (BOC)** establishes the optical interfaces to the detector front end as well as to the **read out system (ROS)** while the **read out driver (ROD)** manages data processing and calibration. Here the first prototype of the new BOC is presented.

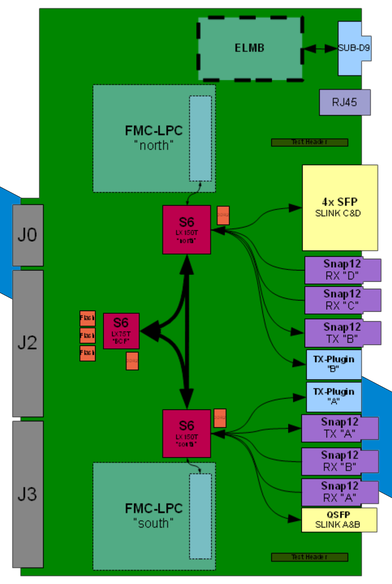
Objective

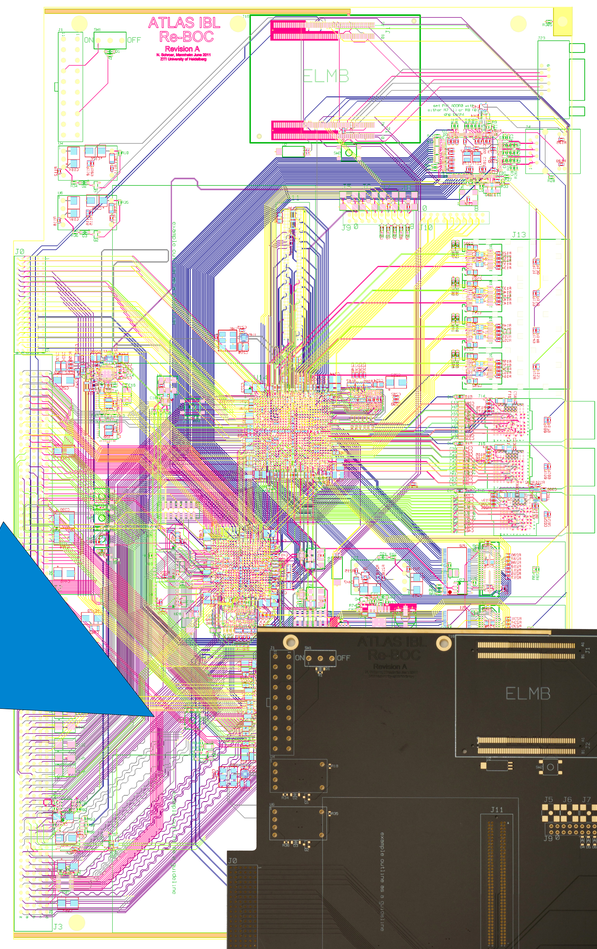
Development of a new BOC to handle the increased bandwidth of the new front end chips while being backward compatible to the existing VME system.



Current BOC

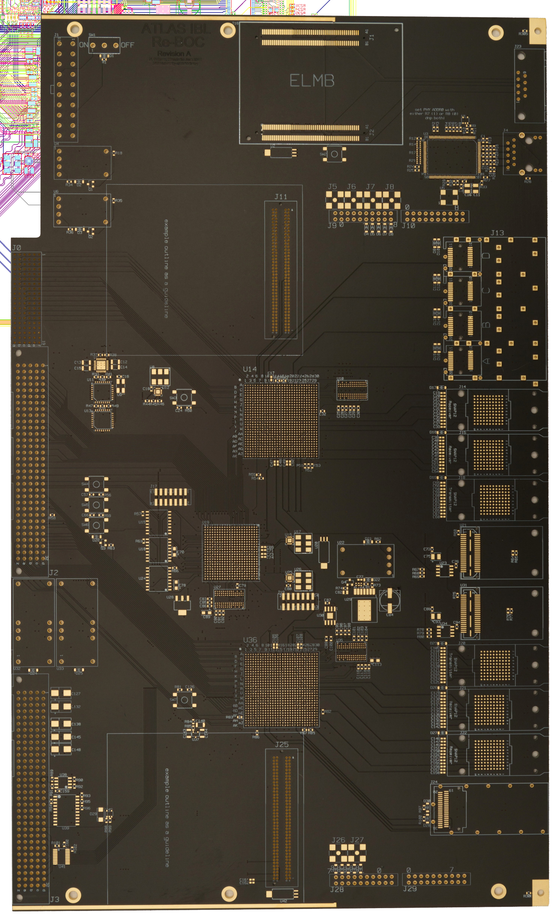
The optical interface to the detector front end is made of custom made plugins for both, the RX and the TX direction. ASICs on the TX plugins manage the BPM encoding of the 40Mbit command streams to the detector and can be used to tune the signal by adding delay, set the mark to space ratio or by changing the laser current for the VCSELs. The RX plugins feature an ASIC (DRX) to receive and amplify the data streams of up to 80Mbit and pass them differentially to the BOC, where the streams are synchronized by custom made delay chips (Phos4). 80Mbit data streams are demultiplexed into 40Mbit before they are passed to the ROD via the VME connector.
Formatted event fragments return from the ROD and are driven to the read out buffer of the ROS via a S-Link mezzanine card (HOLA).





Concept

The idea is to integrate all the functionality of the custom made components into reprogrammable FPGAs while keeping an electrically pin-compatible layout. Commercially available optical transceiver offer flexible usage of different bandwidths. Thus programming the appropriate firmware allows to adapt the BOC to different use cases. A positive side effect is that there is no need to keep custom made hardware in stock for replacements.



IBL BOC Prototype

The IBL BOC handles data from 32 FE-I4 chips (at 160 Mbit each) in two slices of SNAP12 receiver, transmitter and a Spartan6 LX150T FPGA, replacing all the functionality of the former custom made hardware (BPM encoding, synchronization, variable delays). Additionally an embedded S-Link utilizing the high speed serial transceiver (MGT) is implemented to connect to the ROS and a Fast TracKing trigger system (FTK) if needed. The total throughput is 4 times higher compared to the existing BOC, which also requires the ROS interconnect to have 4 S-Link, both SFP and QSFP modules are available on the prototype for evaluation. For the interface to the ROD a so far unused connector (J0) was added and the data rate increased to 80Mbit. Both the Spartans of the two data paths are controlled and configured by a Spartan6 LX75T. New features are a GbE interface, 512Mb of DDR2 memory for each FPGA and an Embedded Local Monitor Board (ELMB) to check temperatures and humidity.
For evaluation and debugging purposes mezzanine card connectors, pin header and LEDs are available.

Status

The prototype PCB is produced and currently being populated with components.
Firmware is developed in parallel and tested on an evaluation board setup until the populated prototype is available in October.

For further information

Please contact *nicolai.schroer@ziti.uni-heidelberg.de*
or visit *www.ziti.uni-heidelberg.de*
More information on the ATLAS project can be obtained at *www.atlas.ch*
or more general at *www.cern.ch*