Contribution ID: **12** Type: **Oral**

The CMS Binary Chip for microstrip tracker readout at the SLHC

Tuesday, 27 September 2011 11:00 (25 minutes)

A 130 nm CMOS chip has been designed for silicon microstrip readout at the SLHC. The CBC has 128 channels, and utilises a binary un-sparsified architecture for chip and system simplicity. It is designed to read out signals of either polarity from short strips (capacitances up to ~ 10 pF) and can sink or source sensor leakage currents up to 1 microamp. Details of the design and measured performance will be presented.

Summary 500 words

The increased luminosity at the SLHC leads to a requirement for increased tracker granularity, and therefore higher channel density. The current CMS tracking detectors need complete replacement and power consumption is a major concern.

The current 0.25 micron CMOS analogue, un-sparsified readout adopted for LHC cannot be translated to SLHC. Off-detector links at SLHC will be digital, and front end digitization of pulse height information would require sparsification to keep data volumes manageable, with increases in system complexity and associated power. We have therefore chosen to implement a binary un-sparsified architecture for short strip readout in the CMS outer tracker, retaining chip and system simplicity at the expense of pulse height information.

The CMS Binary Chip (CBC) has been fabricated in 130 nm CMOS. The chip performance is currently under detailed study, but some specifications which have already been experimentally verified are:
• compatibility with both sensor polarities
• can be DC coupled –up to 1 uA leakage current tolerated
• < 1000 electrons noise for 5 pF sensor capacitance
• power consumption < 0.5 mW / channel

The CBC digital functionality includes pipeline storage of data for up to 256 bunch crossings and provides buffering for 32 triggered events awaiting readout. Critical digital blocks have been designed for SEU resistance. Fast interfaces (clock, trigger, data) are implemented using the SLVS standard. An on-chip bias generator provides the currents and voltages required by the analogue stages, which is programmed via an I2C slow control interface.

CMS has adopted a DC-DC powering solution as the baseline for SLHC, using switching components to translate higher voltages delivered from outside the detector to lower voltage levels required by on-detector electronics. The CBC incorporates features to allow possible powering implementations to be studied. A switched capacitor DC-DC circuit is included which can convert a 2.5 Volt supply to the lower voltage needed by the core circuitry. A low dropout linear regulator is also included which can be used to provide a clean power rail to the analogue front end.

The CBC has been implemented as a 128 channel chip to allow the performance to be studied in a full-size prototype containing most of the features required in a final system.

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Session Classification: A1b - ASICs

Track Classification: ASICs