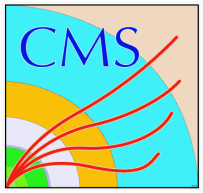
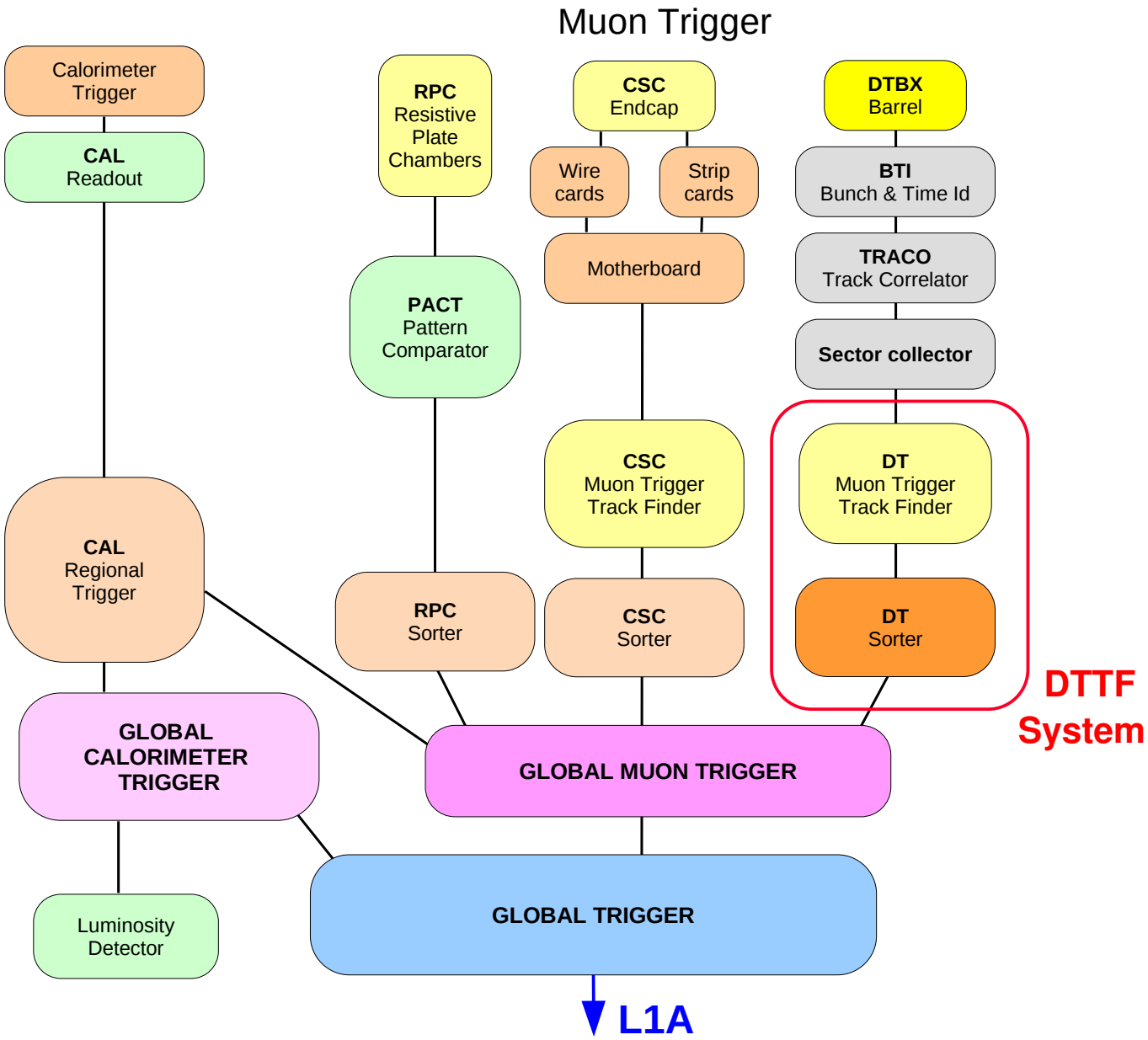


Upgrade plans for the CMS Trigger Drift Tube Track Finder electronics

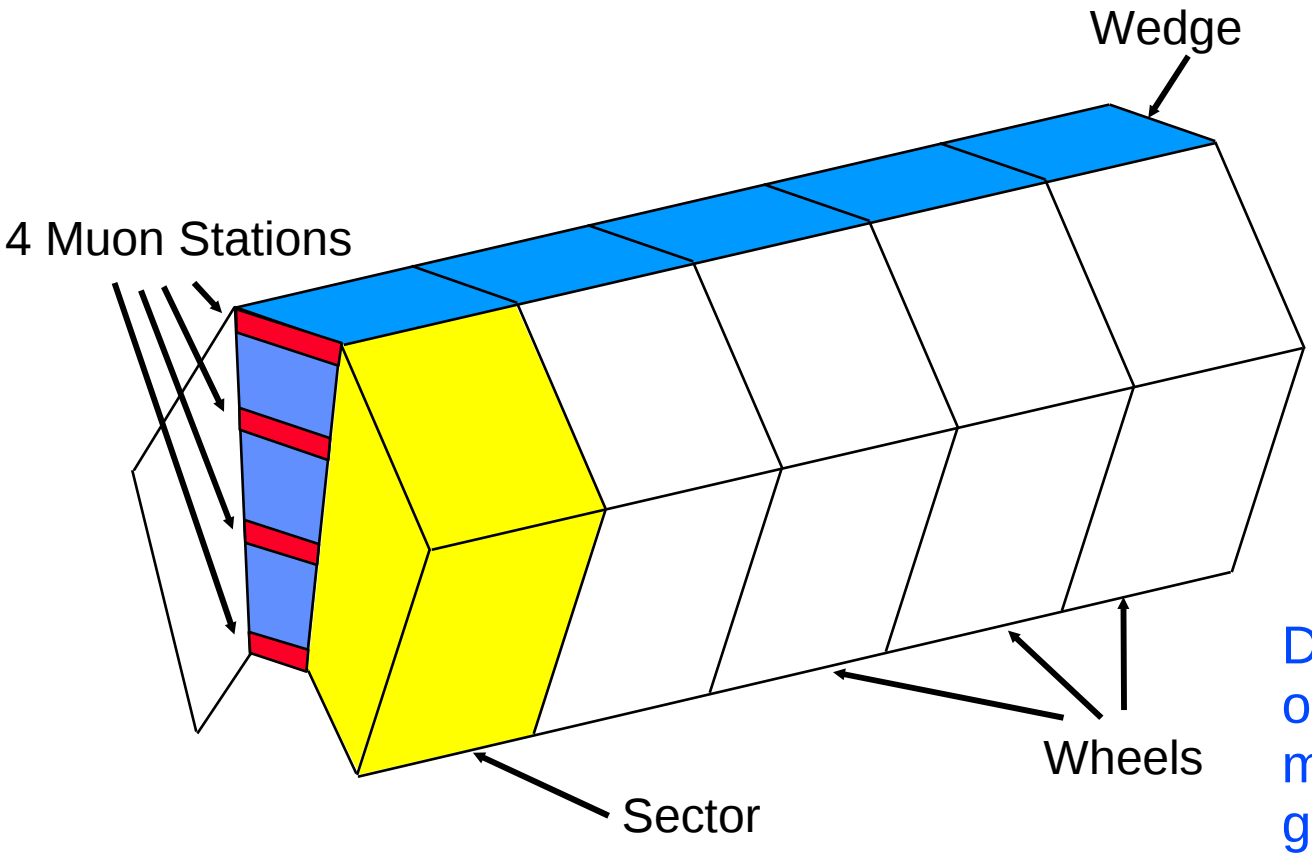
J. Erő
HEPHY/Vienna

DTTF Basics

CMS First Level Trigger Chain



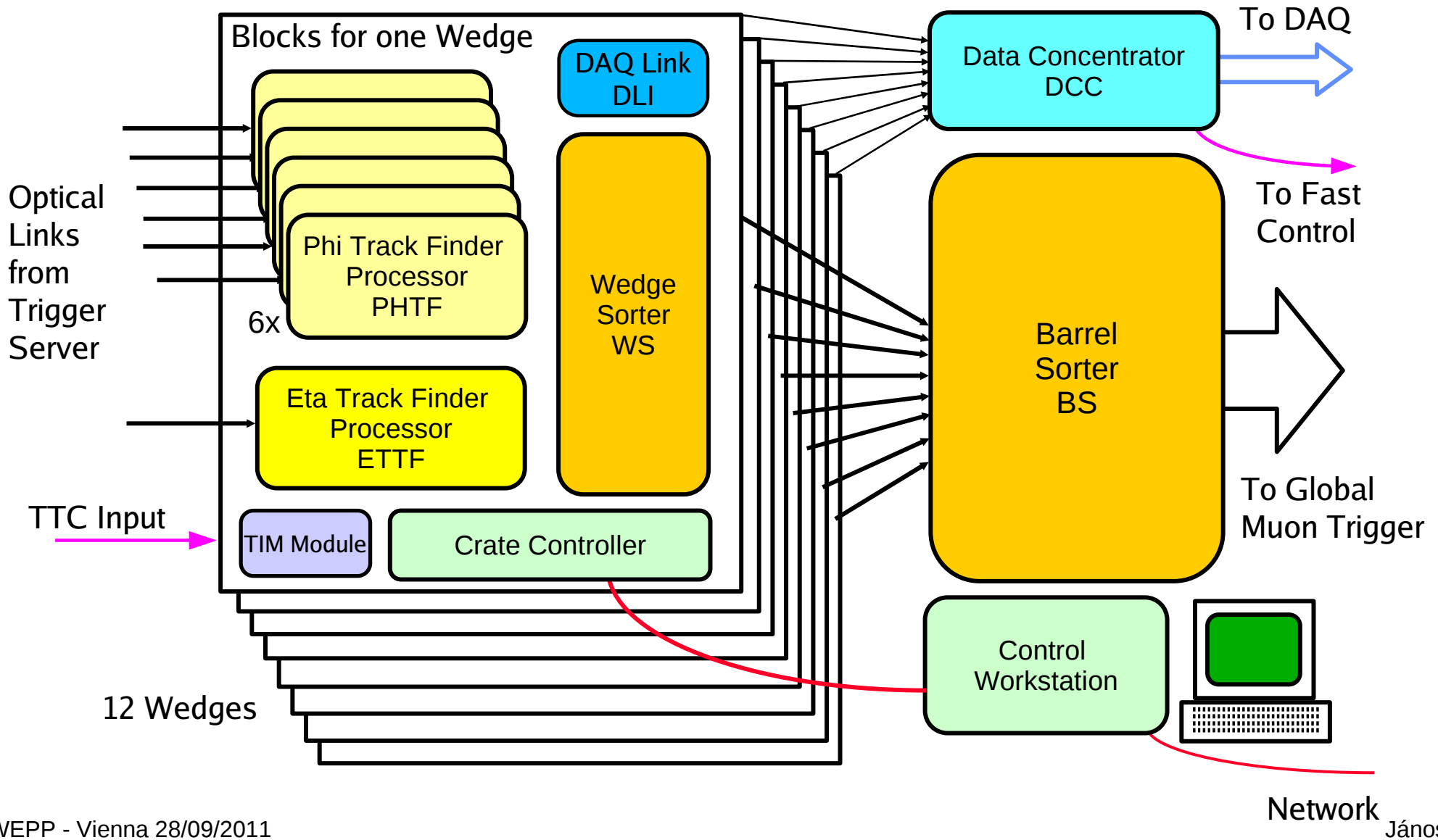
DTTF Mapping



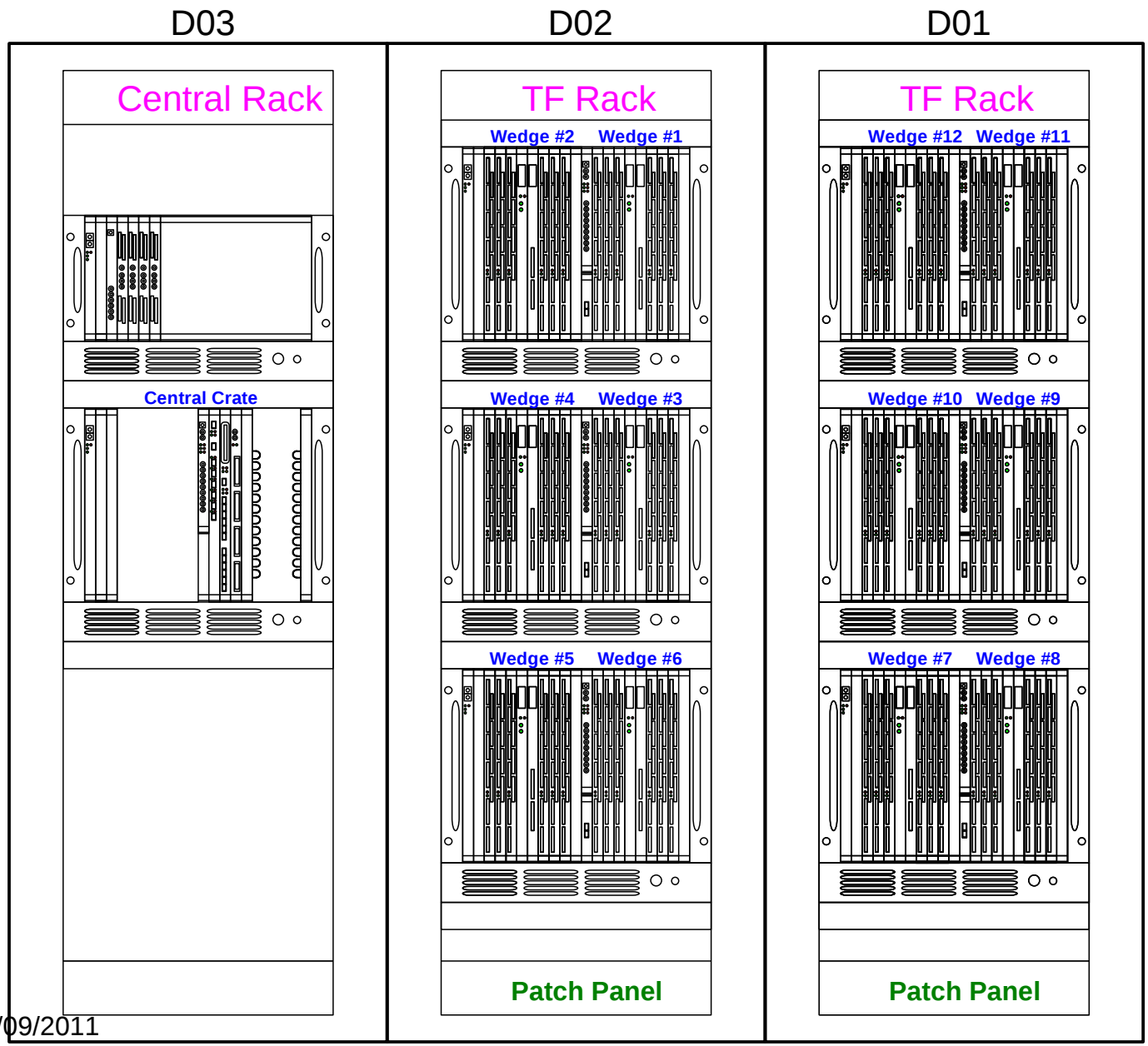
DTTF electronic organized by CMS muon detector Sectors grouped in Wedges

Present DTTF Structure

Sector based



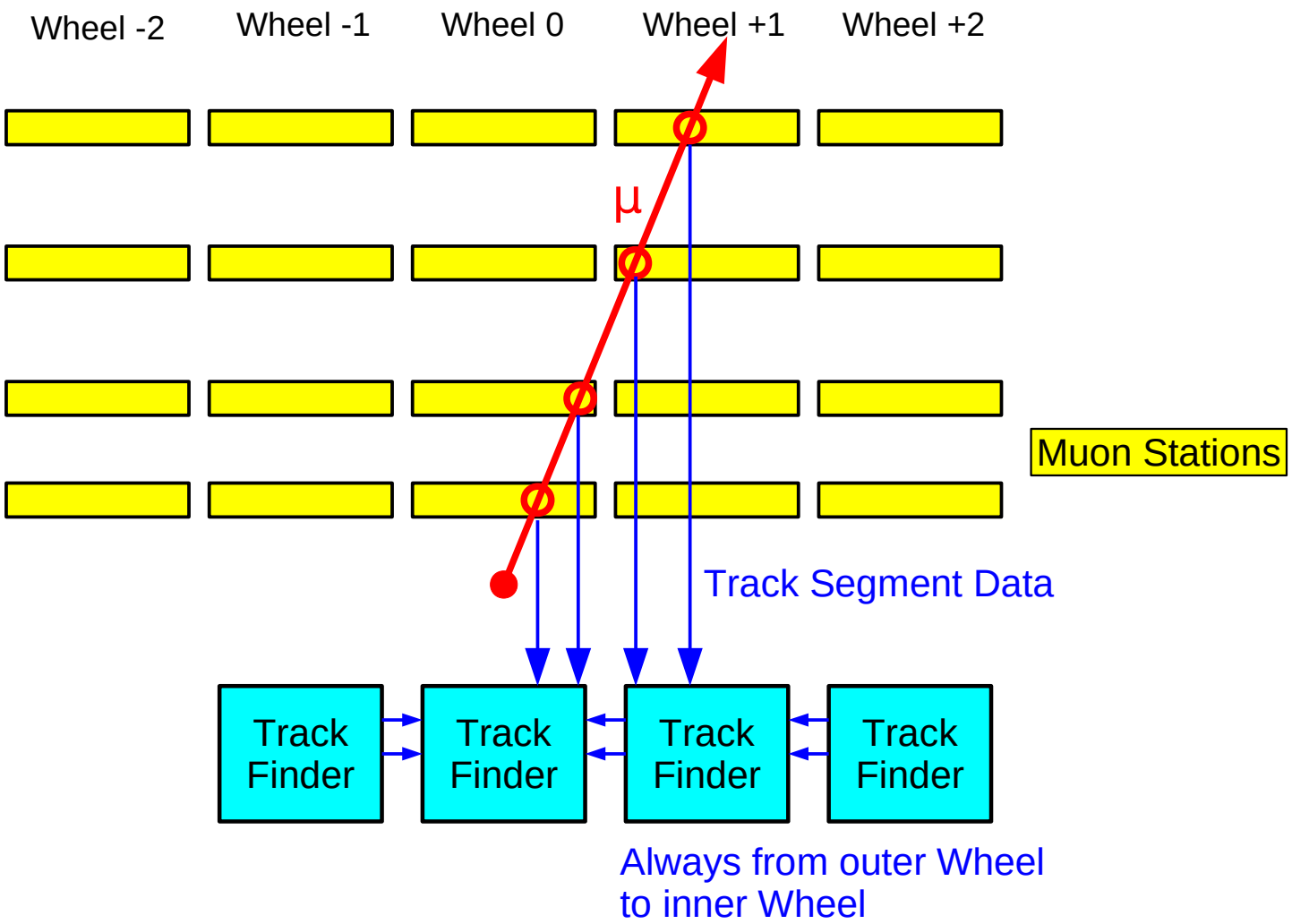
Present DTTF Electronics arrangement



Two Wedges per Crate, VME + Custom Backplane

Neighbour Connections

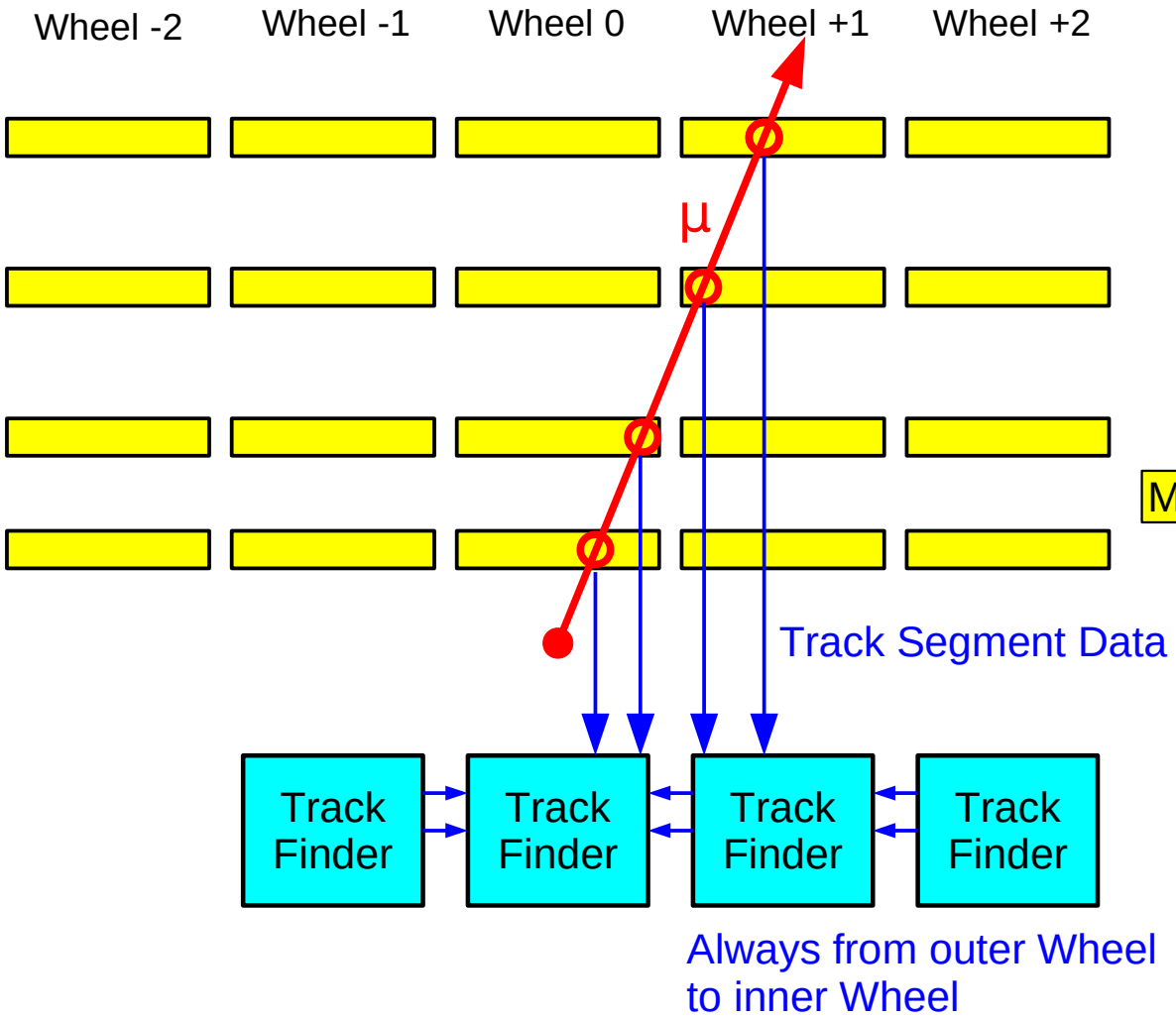
for Muons crossing Sector boundaries



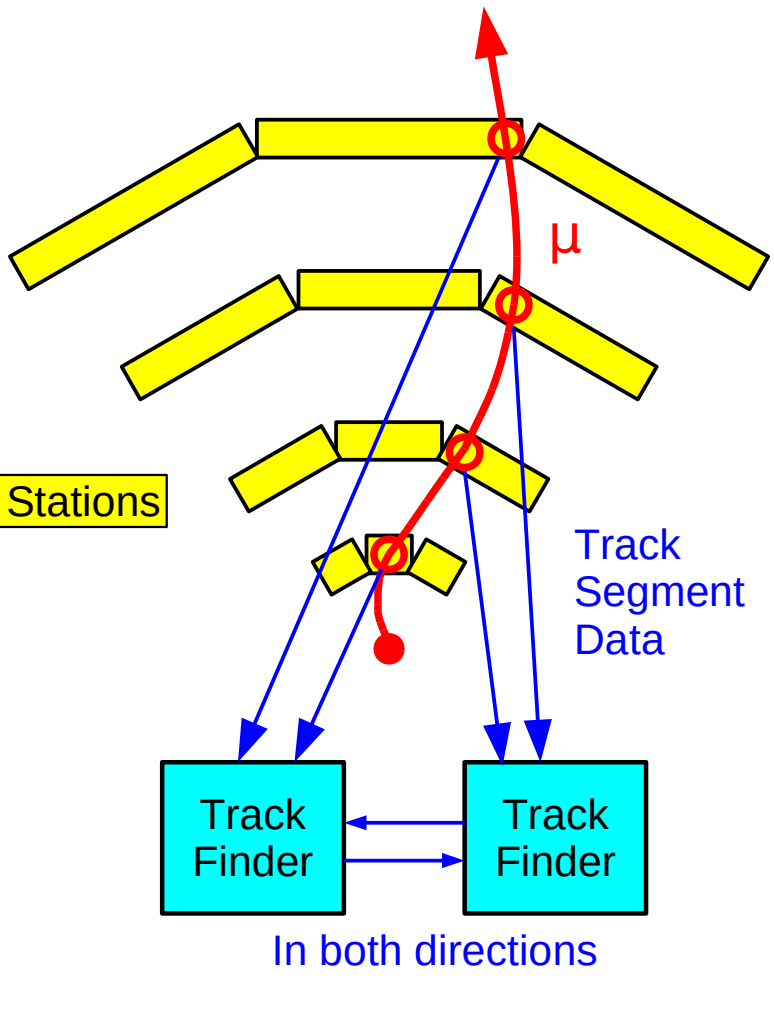
Eta View

Neighbour Connections

for Muons crossing Sector boundaries

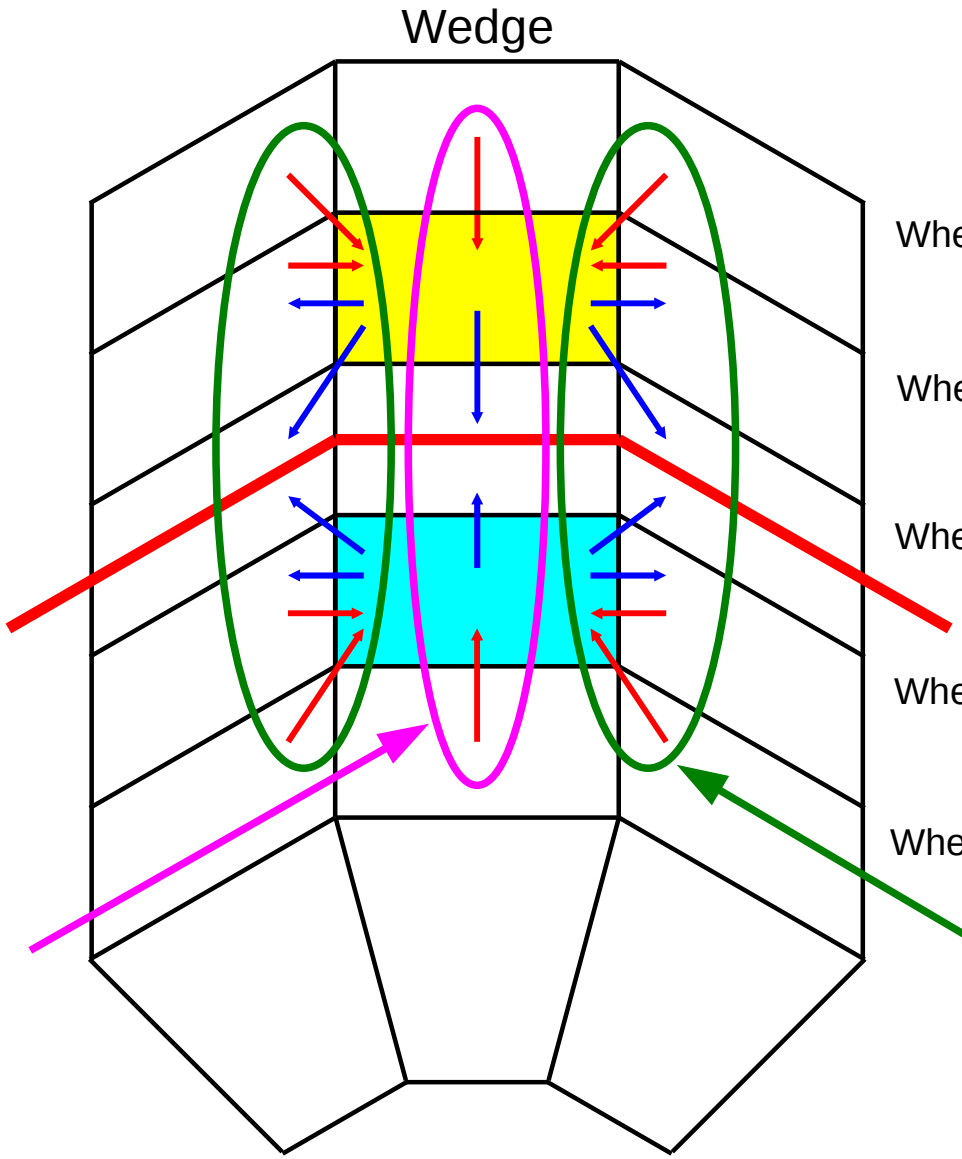


Eta View



Phi View

Neighbour Connections



To minimize L1 Latency all connections parallel !

No connections between positive and negative detector halves!

Data transfer inside Wedge GTL+ signals on the Backplane

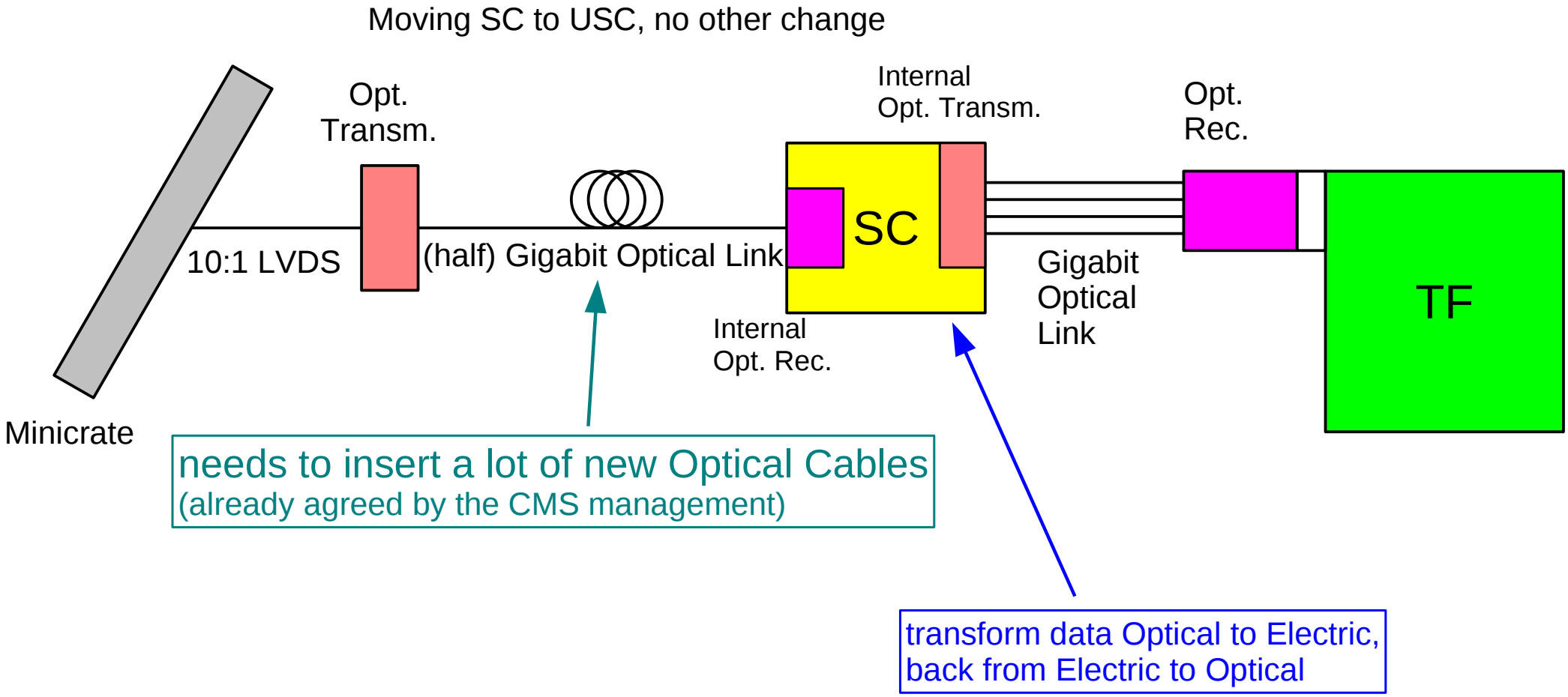
Data transfer between Wedges multi-drop MLVD on flat cables “Green Salad”

The “Green Salad”

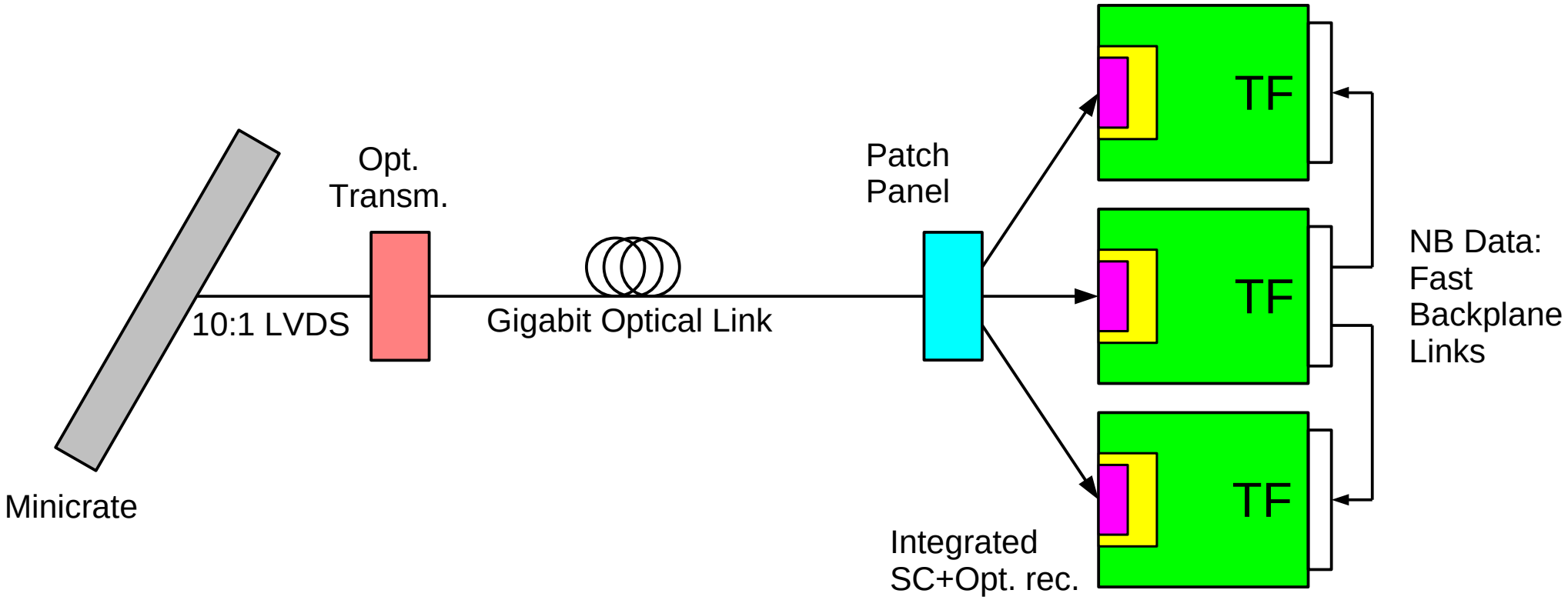
120 output connectors
7680 output pins
432 input connectors
27'648 input pins

A Maintenance Issue

SC to USC
(shown Trigger Chain only)

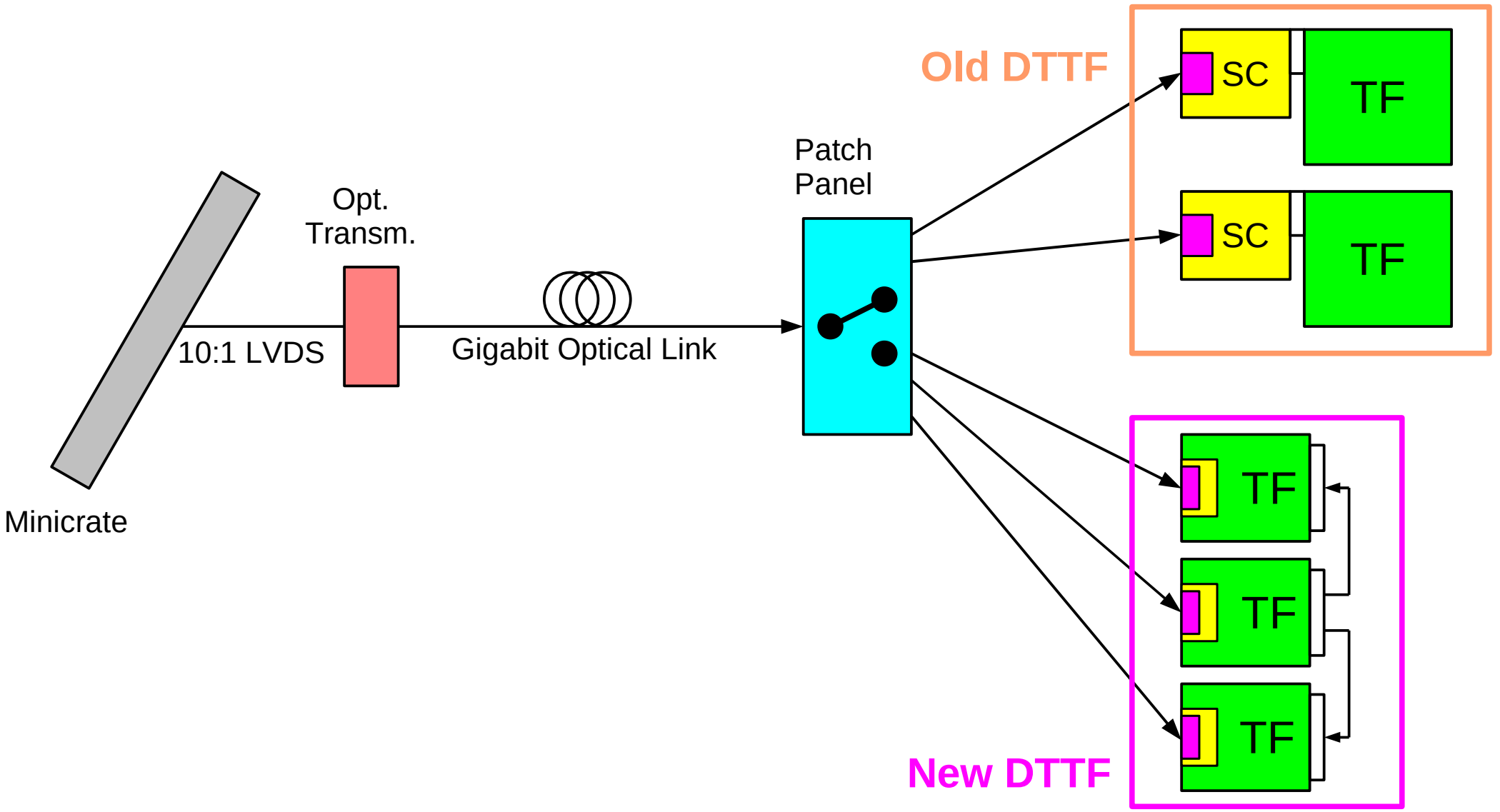


Trigger Object distribution on Backplane



Trigger Object distribution through fast serial Links (µTCA)

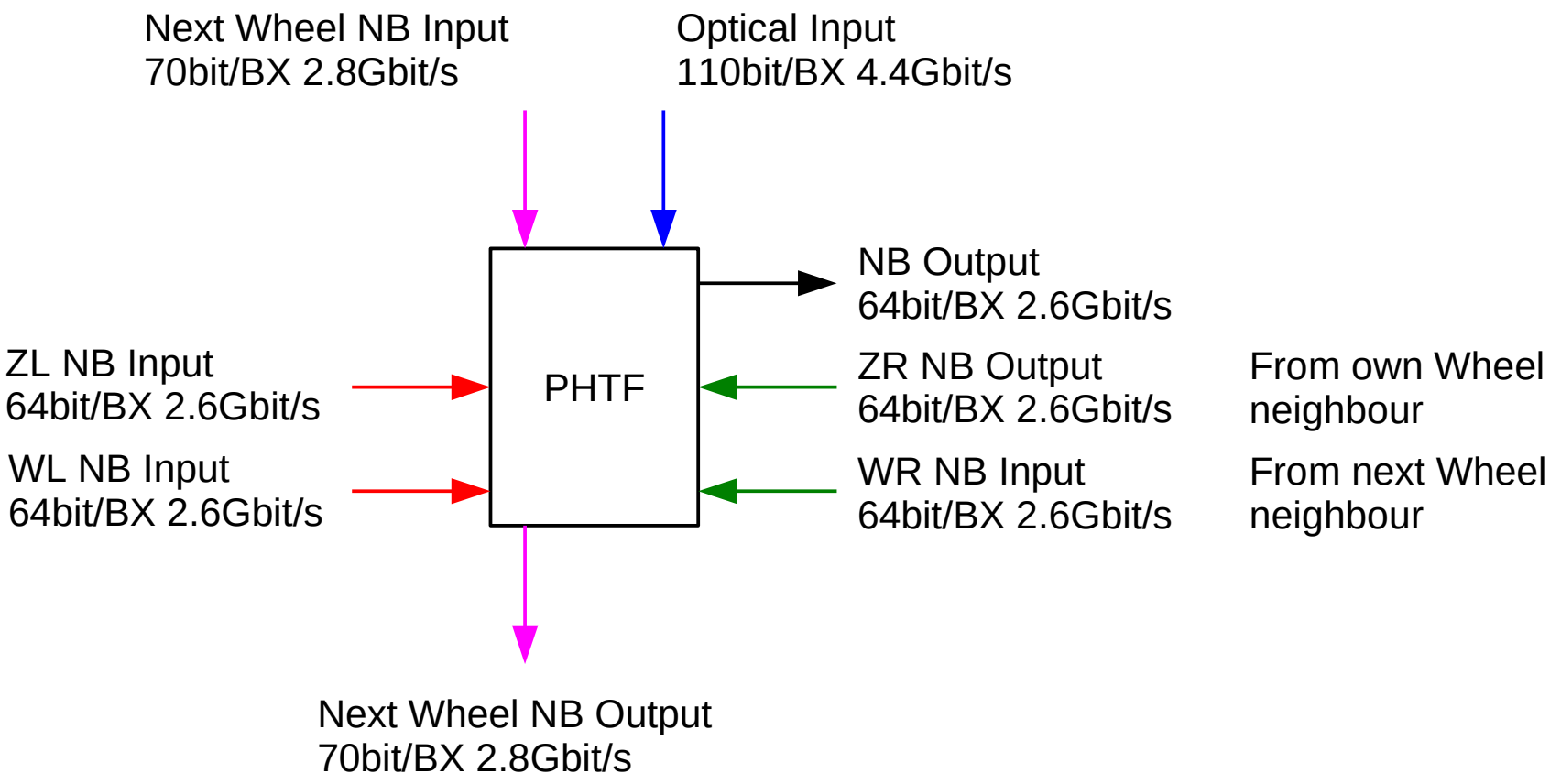
Trigger Object distribution on Backplane



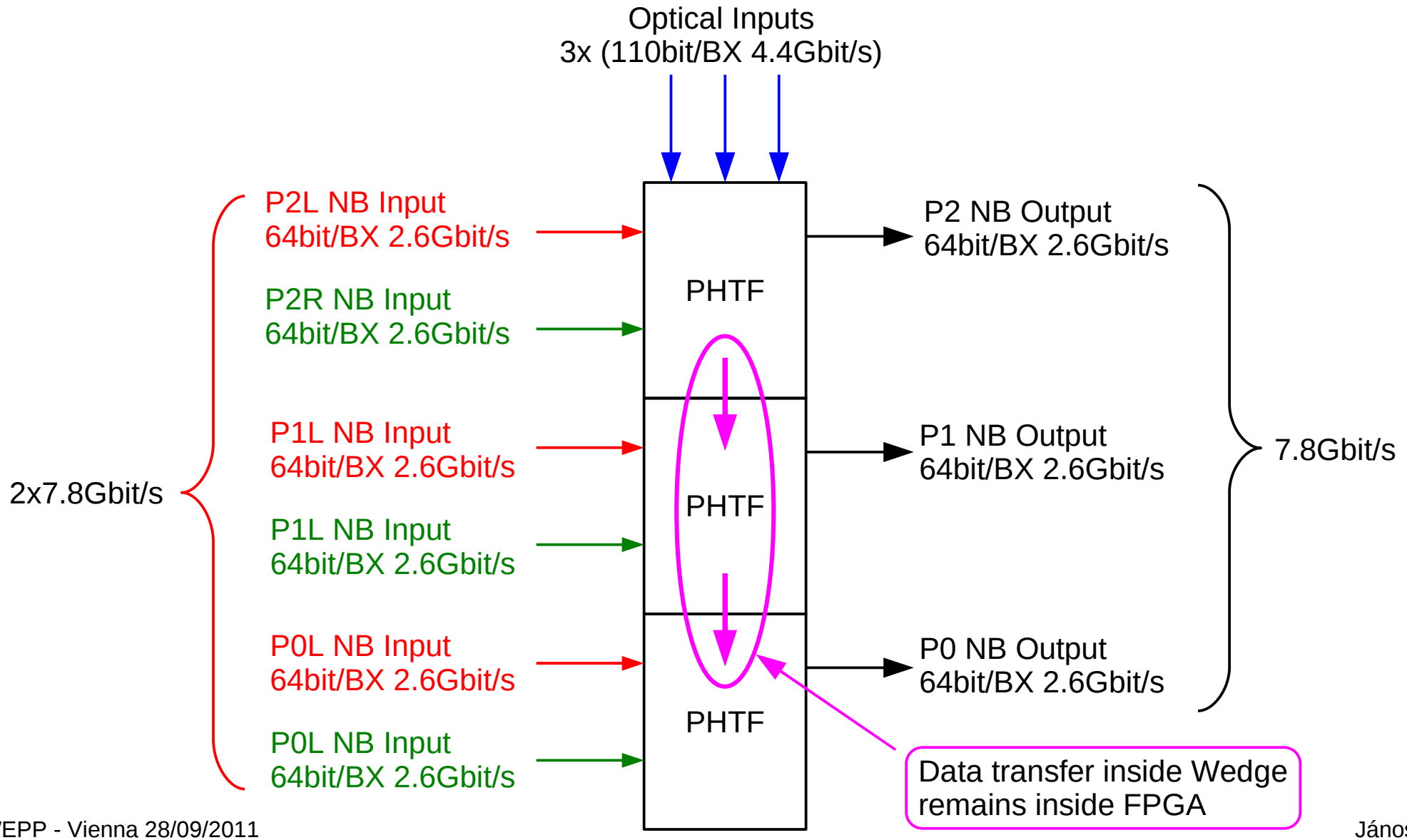
Baseline for Upgrade

- Technology goal: improve connections, reduce failure rate
- Put more logic into one Card (FPGA)
- Use Backplane connections instead of cables
- CMS: 12 DT Sectors – µTCA: 12 AMC Slots in one Crate
  - a half Wedge seems to be optimal
- Use CMS feature of independent Positive and Negative detector halves
  - Data from Wheel 0 must be shared between units serving Half Detectors
- Input data “as is”
  - new SC compatible with old one
- Use CERN background
  - central services and S/W development
    - DAQ, TTC can be of common design
    - HAL service must be taken!
- Smaller system costs less
  - 2 Crates, 24 TF Boards + Sorters

PHTF Sector I/O Bandwidth



I/O Bandwidth when Merging a half Wedge (0-1-2 Wheels) into one FPGA



Logic Resource Requirements

- Present PHTF
  - Inrec chip
    - LEs: 7100
    - Mem: 106 kbit
  - SOC chip
    - LEs: 30'700
    - Mem: 834 kbit
- Present ETTF
  - Inrec_et chips (5)
    - LEs: 2750
    - Mem: 23 kbit
  - Etsoc chip
    - LEs: 14'400
    - Mem: 320 kbit

- 3 Sectors in one Board
- 3xPHTF + 3/5 ETTF
  - Inrec chip
    - LEs: 29'550
    - Mem: 387 kbit
  - SOC chip
    - LEs: 100'740
    - Mem: 2'694 kbit

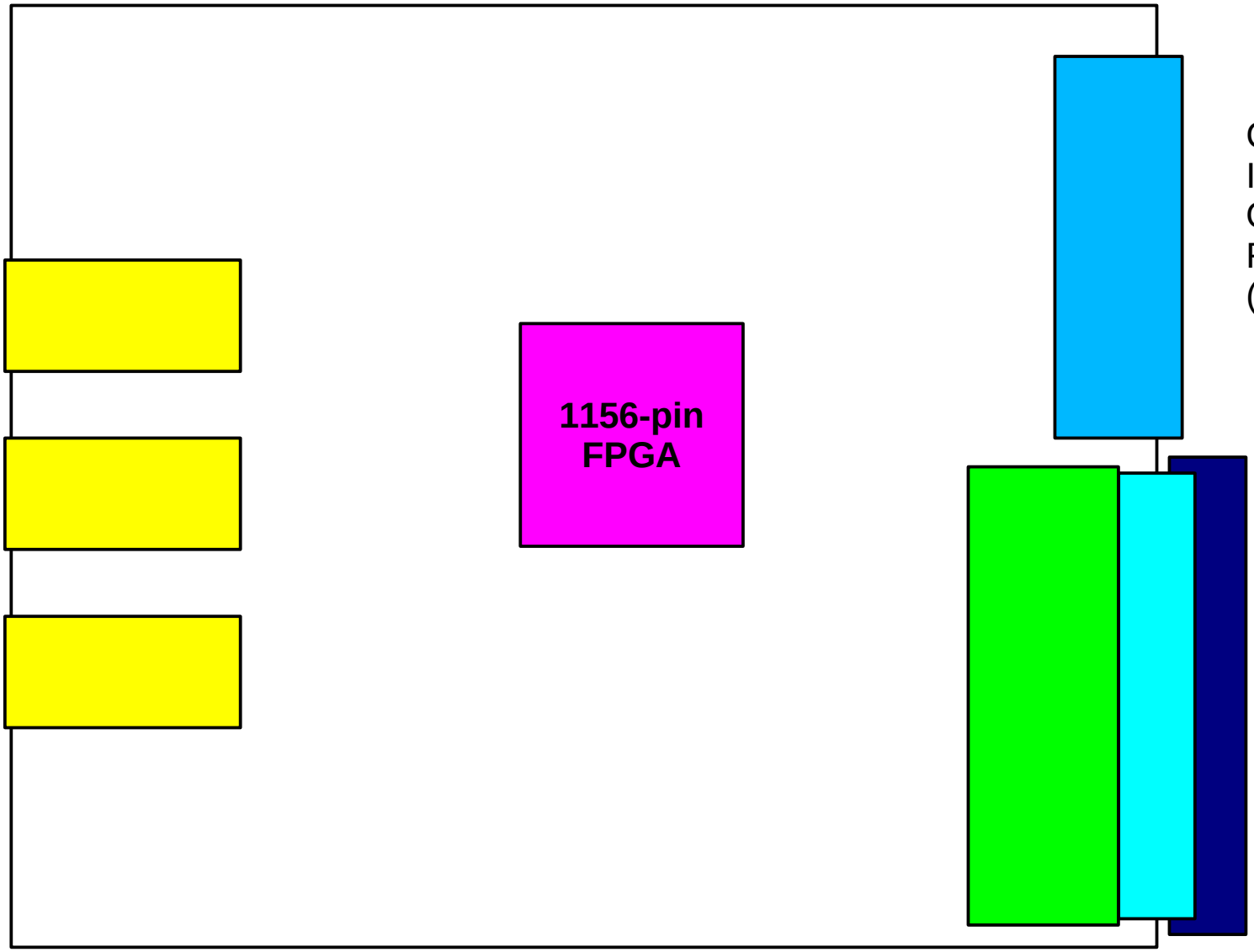
LEs: 130'290
Mem: 3'081

- Trigger Input
  - 18 fibers - Serdes (1.28 Gbps)
- Fast Links (lanes)
  - Neighbour Data
    - 3 output fast Links (2.6 Gbps net)
    - 6 input fast Links (2.6 Gbps net)
  - Trigger Data
    - 1 output fast Link
  - DAQ Data
    - 1 output fast Link

Feasibility 3.
Available FPGAs

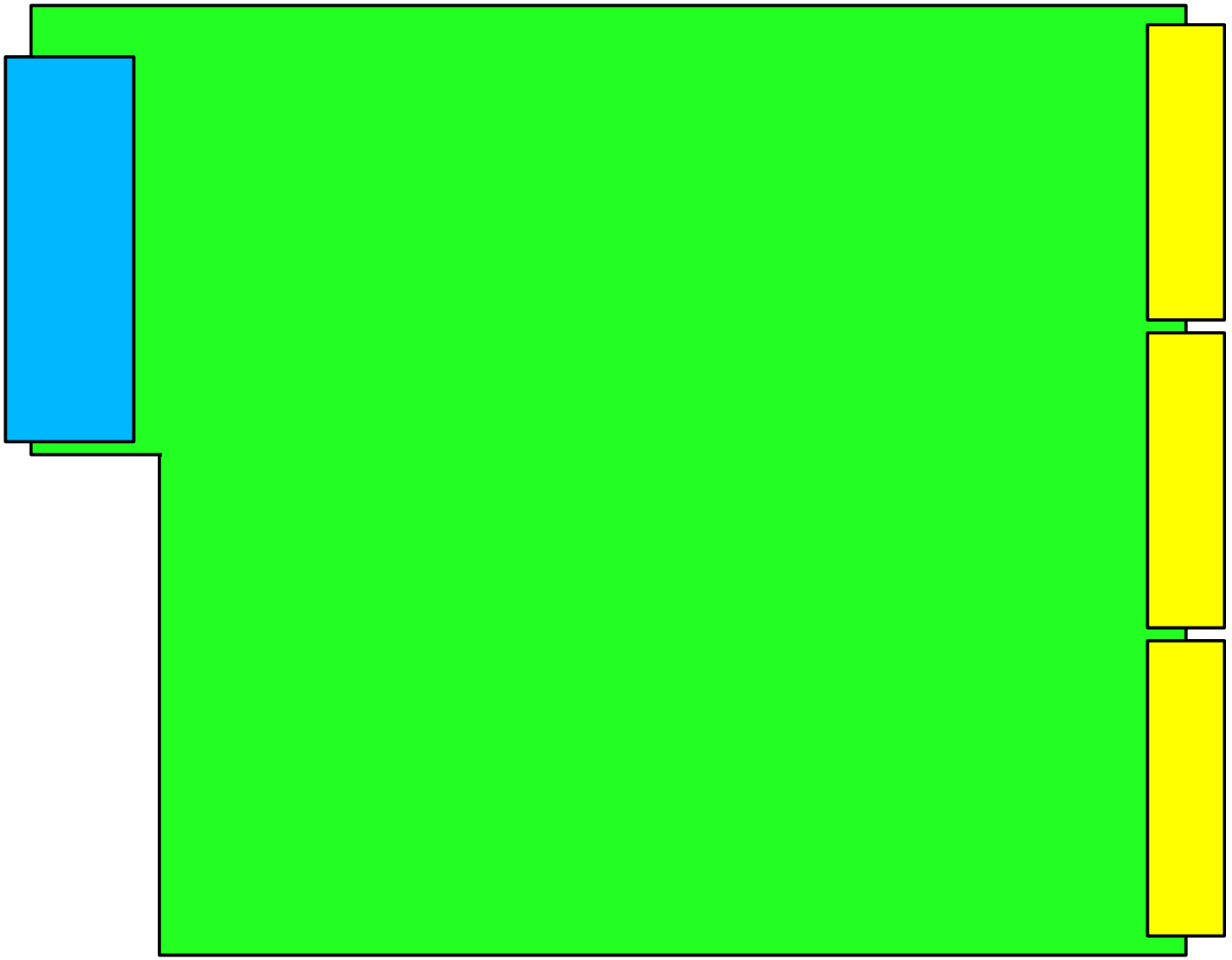
FPGA family	FPGA type	Subtype	speed	Pincount	Price EUR	LE	Memory kbit	I/O pins	PLLs	SERDES number	SERDES speed (Mbps)	GTX number	GTX speed (Gbps)
ALTERA													
Stratix 4	EP4SGX110	GX	-4	1152	2000	105,600	9,564		4	28+28	1600	16	0.6 – 8.5
Stratix 5	EP5SGXA3	GX	-4	1152		200,000	16,000	552		156	1400	24	14.1
Arria 2	EP2AGX190	GX	-6 -4	1152	1211 1696	181,165	9,939	612	6	145	1250 1250	16	0.155 – 6.375
Arria 5	EP5AGXA5	GX		1152	???	190,000	11,800	544		120	1250	24	0.600 – 10.31
XILINX													
Virtex 6	XC6V195T	LXT	-1	784	914	199,680	12,386	600	10	200		12	0.48 – 6.6 ?
	XC6V195T	LXT	-3	784	1600							12	0.48 – 6.6
	XC6V195T	LXT	-1	1156	1050	199,680	12,386	600	10	300		20	0.48 – 6.6 ?
	XC6V195T	LXT	-3	1156	1850							20	0.48 – 6.6
	XC6V240T	LXT	-1	1156	1300	241,152	14,976	600	12	300		24	0.48 – 6.6 ?
	XC6V240T	LXT	-3	1156	2260	241,152	14,976	600	12	300		24	0.48 – 6.6
Artix 7	XC7A175T			784	???	173,120	6,660	450	9	216		4	3.75
Kintex 7	XC7K160T		-3	676	???	162,240	11,700	200	8	192	1600	8	0.5-12.5
	XC7K325T		-3	900	???	326,080	16,020	350	10	240	1600	16	0.5-12.5
	XC7K325T		-2	900	???	326,080	16,020	350	10	240	1400	16	0.5-6.6
Virtex 7	XC7V285T	T		784		286,080	14,760	350	14	~170		12	12.5
				1157		286,080		600	14	~280		20	12.5

TF AMC Board Layout study

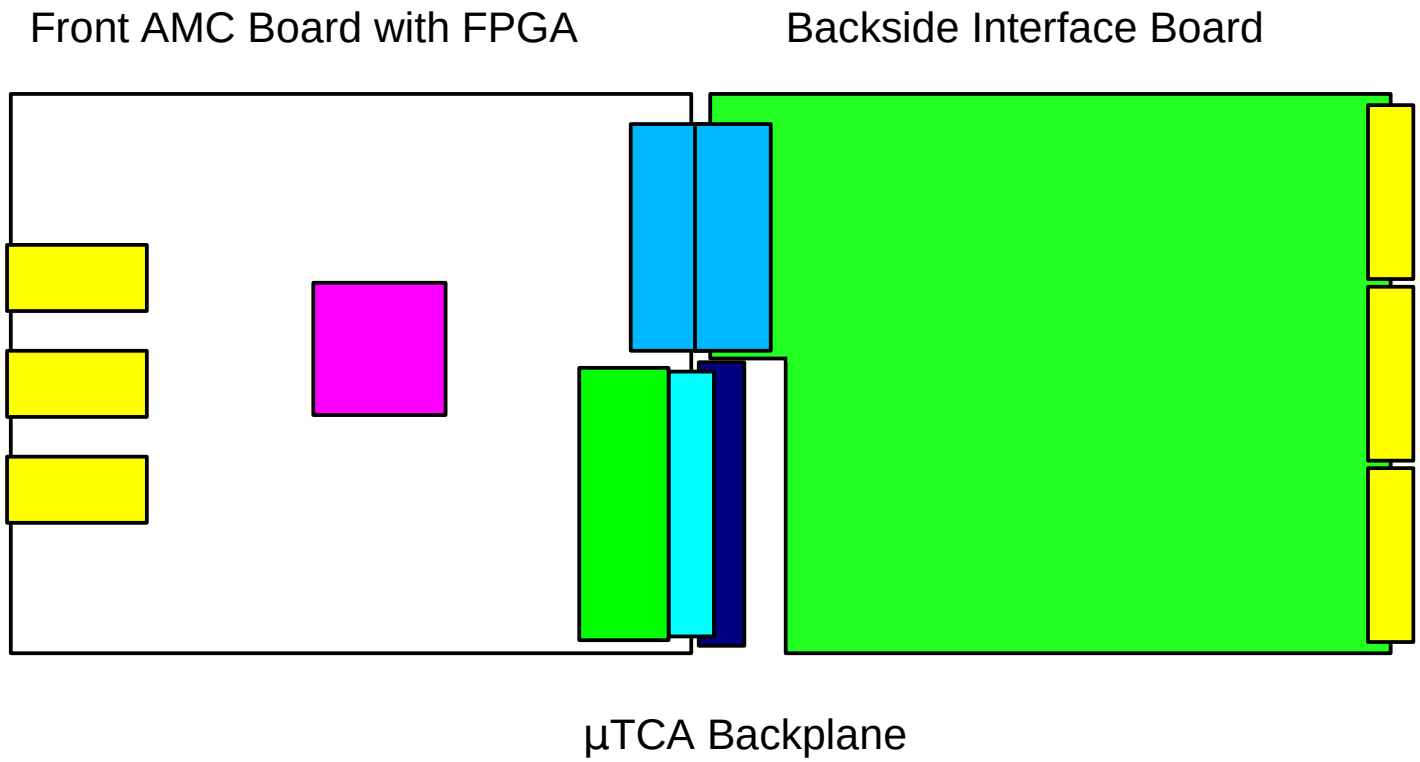


Scale = 1:1

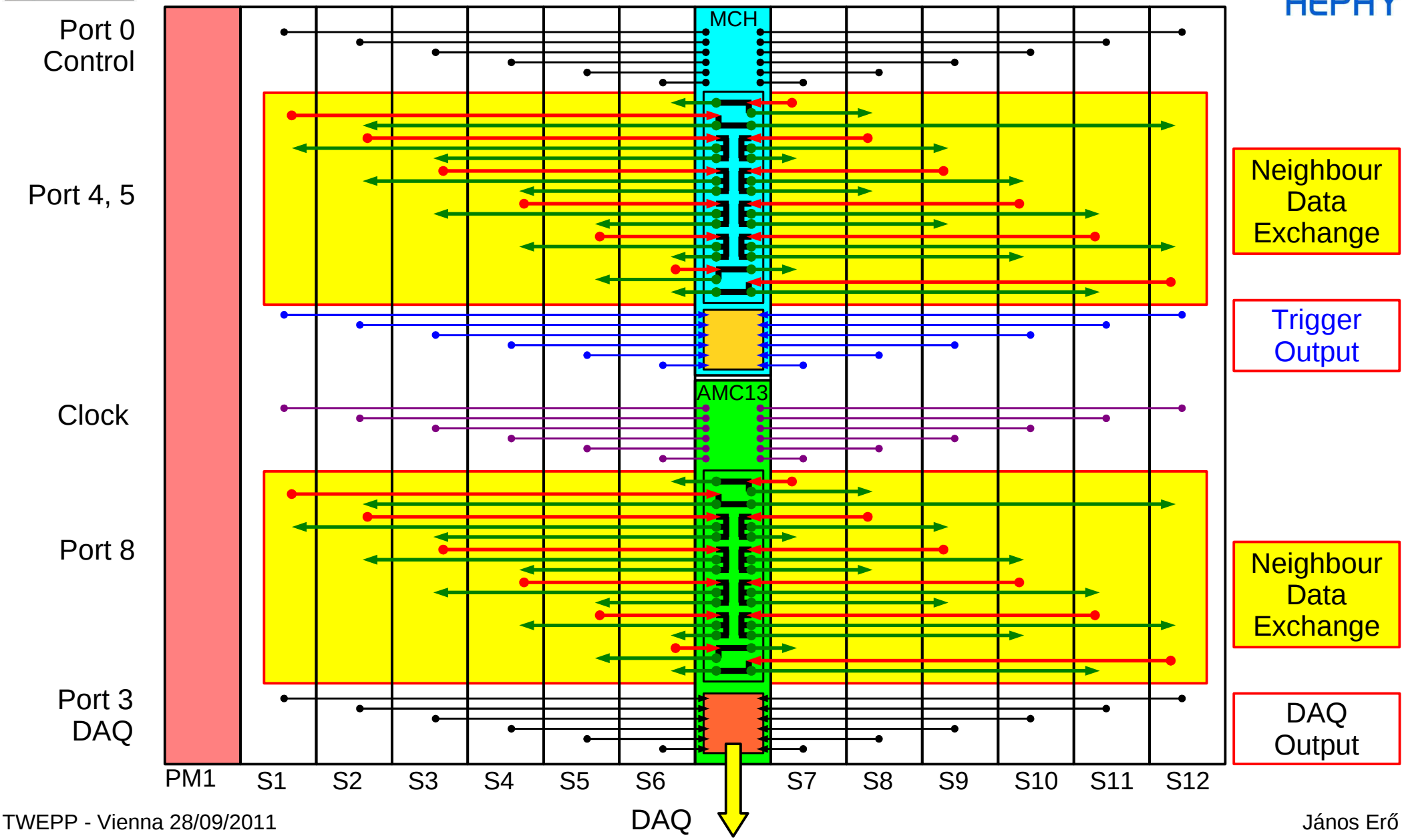
Backside Board for CSC Inputs



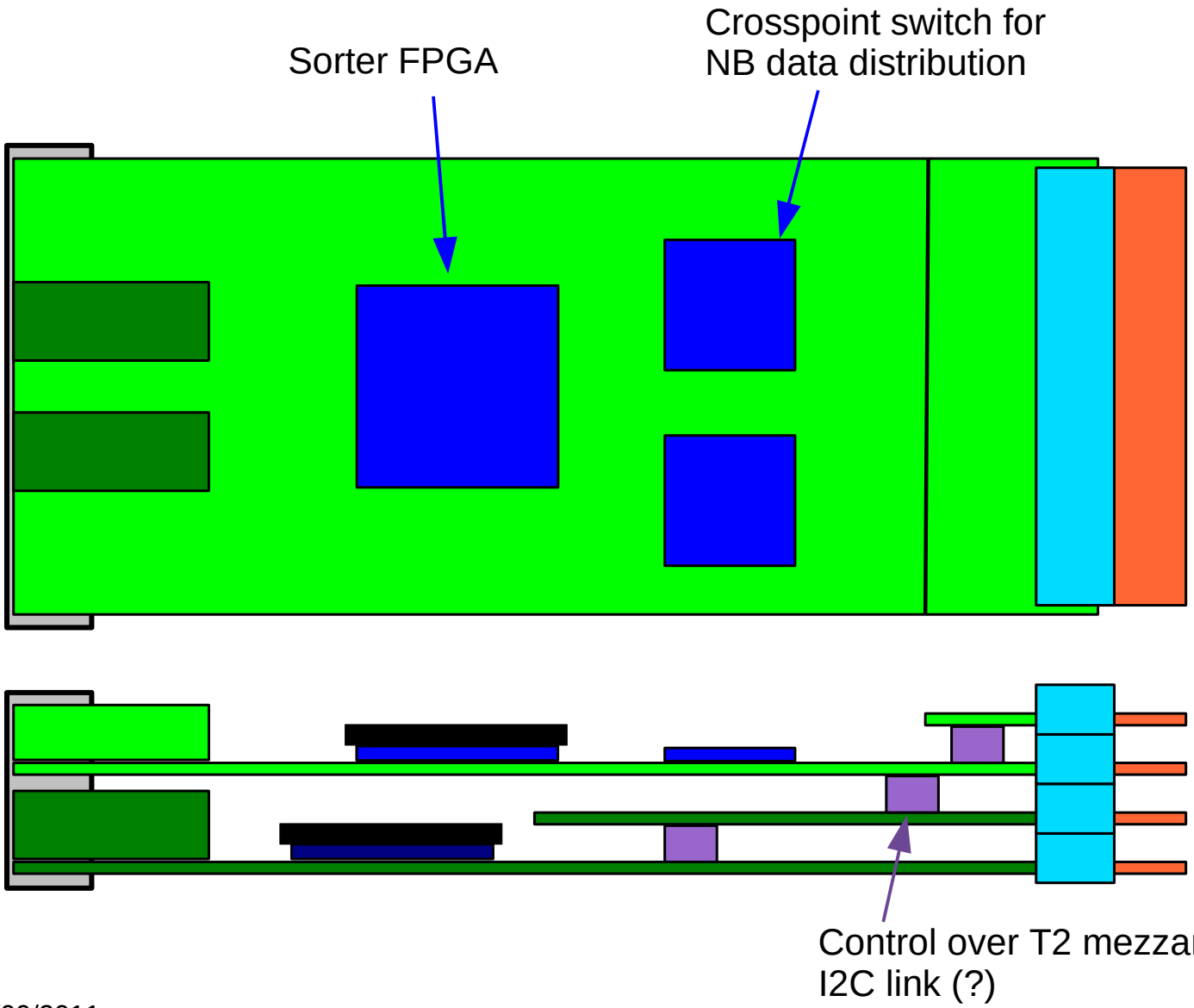
Dual Board System



With Standard Backplane (Vadatech VT891 opt.)



Data Fanout as MCH & AMC13 mezzanine

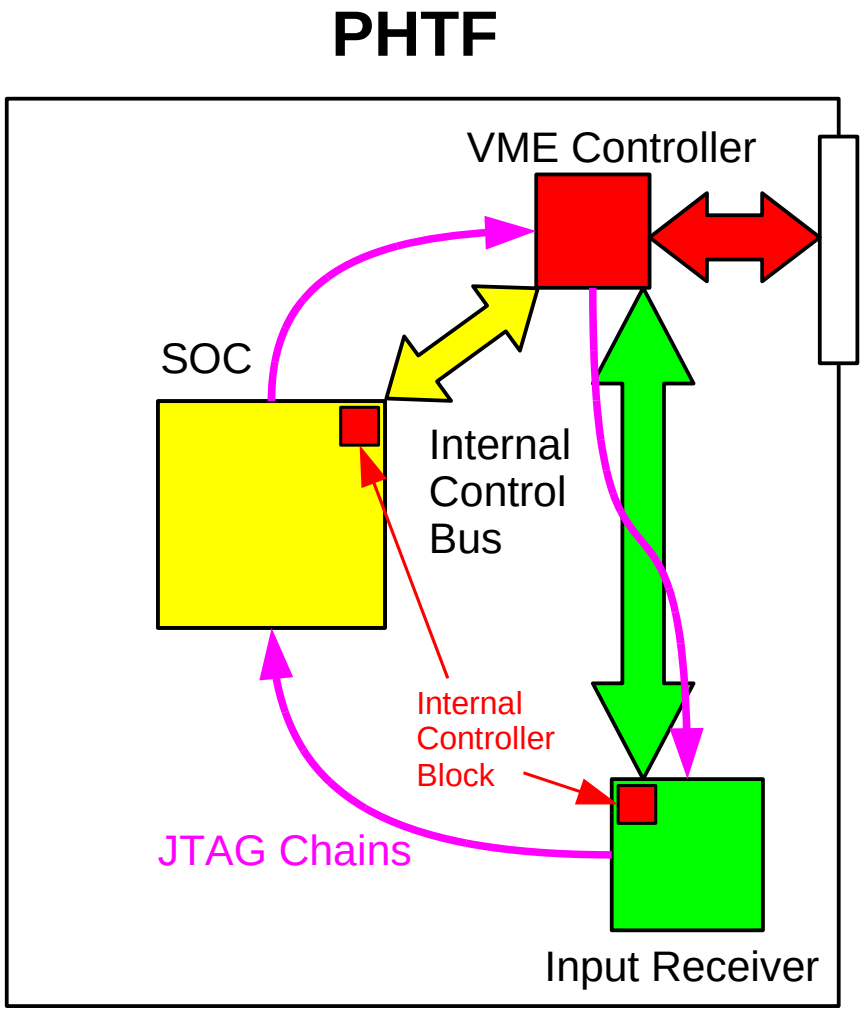


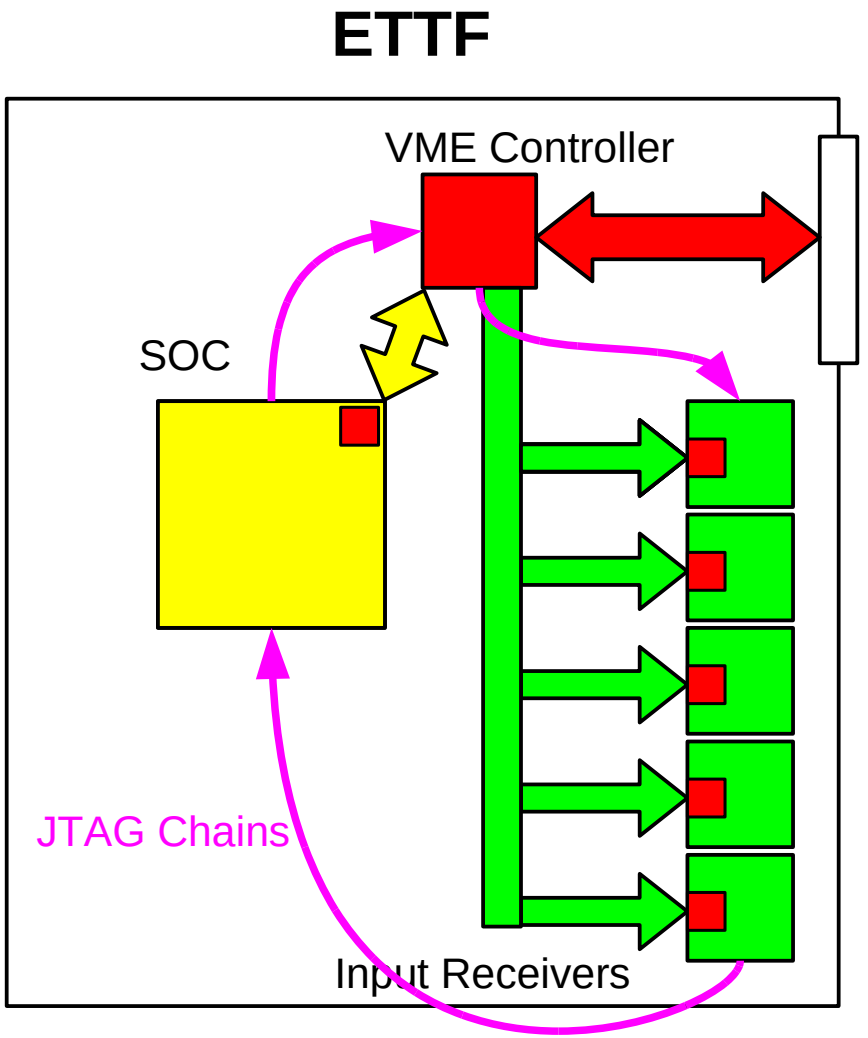
Two Boards as MCH and AMC13 side fanout

- MCH version
  - MCH compatible mezzanine conn.
  - 2x12 → 24 Lanes Fanout
  - No FPGA
  - Compatible with MCH Front Panel
- AMC13 version
  - AMC13 compatible mezzanine conn.
  - 12 → 24 Lanes Fanout
  - Sorter FPGA
  - Trigger Output
  - Copy of AMC13 LED & JTAG I/F

- Simplify design
  - Mezzanine connector might be different – keep similar sections
  - Crosspoint switch and FPGA part might appear in both
  - Front Panel section possible common

Present DTTF Control Structures

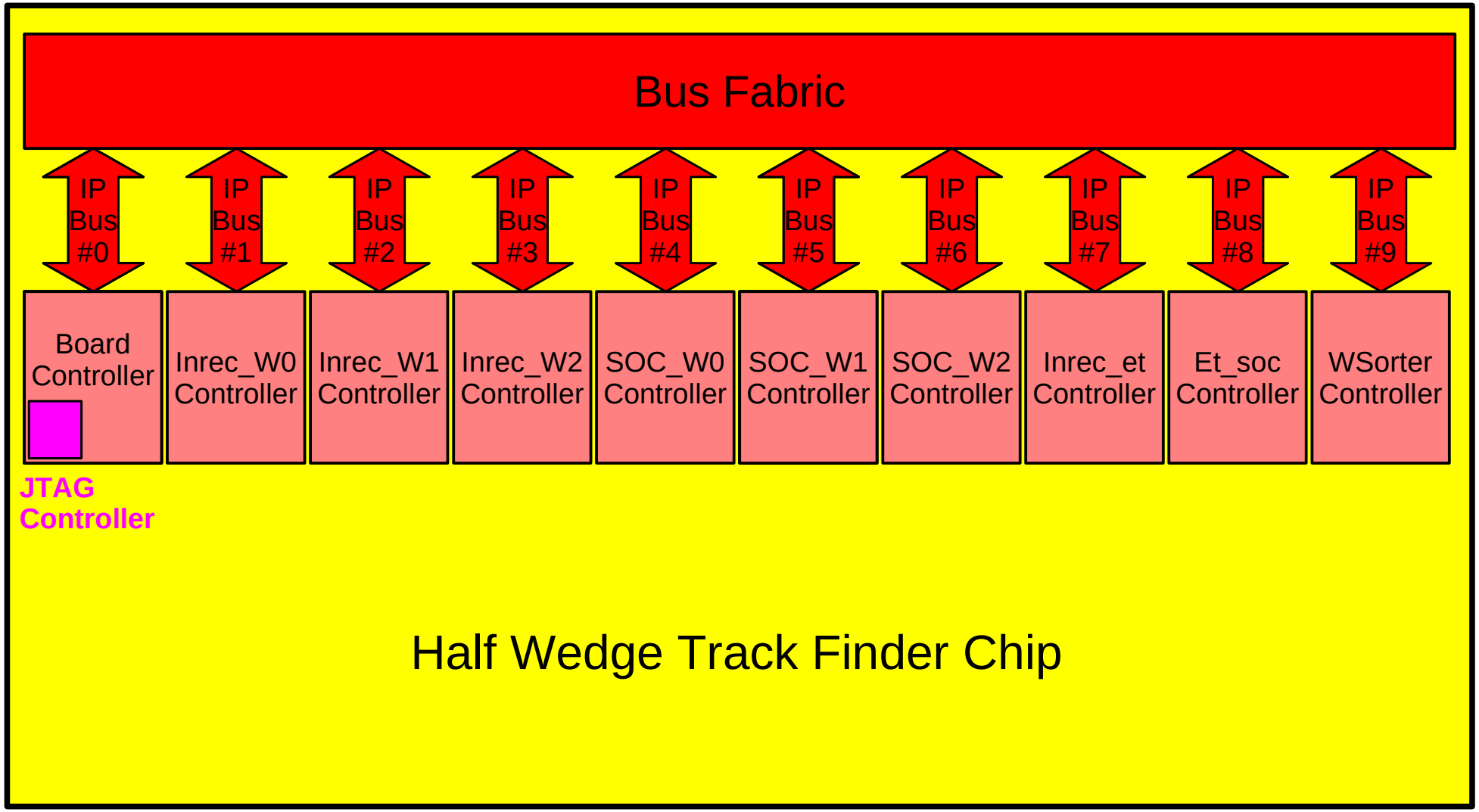




Goals for a new Control Scheme

- Design for merging 3 PHTFs and a half ETTF
- Keep present control structures
  - allows using existing Firmware VHDL blocks
  - simple merge scheme
  - small changes for maintenance programs and simulation data
  - easier application control programs
- Map control structures into **IPbus**
  - CMS support
  - existing mapping scheme
  - use the same Entity for all control functions
    - synthesis optimizes parallel structures away

New Track Finder IPbus Structure



Feasibility Study, Prototyping

- Open Questions
  - Bandwidth Fitting
    - Trigger Object distribution
    - DAQ Output
    - Trigger Output
    - Control
  - Optical Link Questions
    - Multi-Fiber Optical cables & connectors
      - Place and routing requirements
    - Patch Panel and/or Optical Splitting (Wheel 0)
  - µTCA developments at CERN
    - Custom Backplane options
    - DAQ output Options
    - Control Options
    - TTC Options

Collaborations, Schedule

- CERN
  - CMS µTCA developments
  - Common fields
    - TTC, DAQ interface
    - Fat Pipe usage
    - Gbit Switch technology
    - Software (HAL)
- Vienna
  - Global Trigger + Muon Trigger into µTCA
  - Trigger Supervisor
- DT Collaboration
  - SC + Optical Input

- Newest LHC operation schedule not optimal for Upgrade
  - 2014 shutdown: too early
  - 2019 shutdown: too late
- Parallel operation for old and new DTTF
  - Technology demonstrator – Dec. 2011
  - Prototype Boards – 2012, 2013
  - Production System – 2015
  - Commissioning - 2016,2017