Open Hardware
for CERN's Accelerator Control Systems

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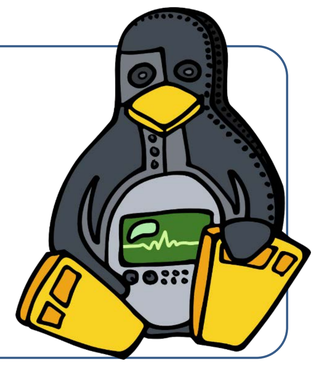
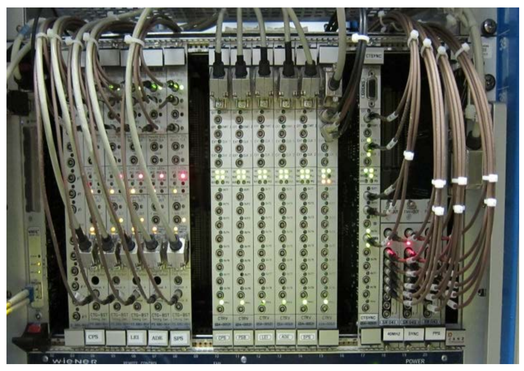


Overview of BE-CO Controls Hardware

- The Controls Group of the Beams Department (BE-CO) at CERN is responsible for the specification, design, procurement, integration, installation, commissioning and operation of the controls infrastructure for all CERN accelerators, their transfer lines and the experimental areas.
- The group provides services like general machine and beam synchronous timing generation and distribution and signal observation systems, as well as support for drivers and higher-level software.
- As example, Quench Protection, Cryogenics, Power Converters and other critical systems use BE-CO's kit. The screens in the CERN Control Centre are generated using BE-CO's hardware and software.



Timing crate controlling LHC

- Around 120 module types are supported (stock, repairs, drivers).
- Three out of four module types are custom designed; one in four is commercial.
- One in four module types is obsolete: they can be repaired, but cannot be ordered or re-produced.

Need for Open Hardware

Using commercial modules saves effort as they are designed, built and tested already. Unfortunately, ready-made modules don't always have the exact functions we need. E.g., even for simple ADC modules CERN needs specific trigger modes or input capabilities that are not usual. Furthermore, when a bug is found, it may be hard to get a correction from the company as CERN's applications are very complex and the reported bugs may be difficult to reproduce. Ultimately, as there is normally no access to design documentation, it is impossible to help in solving problems. We believe we have found a way to combine the advantages of both commercial and custom hardware by using the concept of "Open Hardware", similar to the concept of "Open Software".

The main ideas behind the Open Hardware paradigm are:

- All specifications and design files are published: benefit from peer review and enable remote collaboration.
- All detailed production files for the hardware, including PCB production files, precise bill-of-material and assembly instructions are published so that anyone can reproduce the hardware.
- Peer reviews are actively sought for to improve the designs and to make them better re-usable.
- Companies may produce, sell and support the open designs like products of their own.

Standards for New Designs

To ease design work, maintenance and to guarantee longevity, new designs are based on standards.

External bus standards

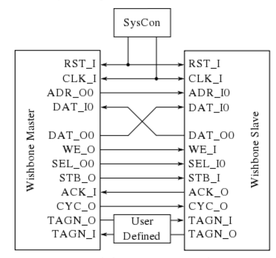
- VME64x
  - Boards with 6U height and large front-panel space
  - Possibility of using Rear-Transition Modules
- PCI Express
  - Used in PICMG 1.3 industrial type PC

FMC Mezzanine bus standard

- FPGA Mezzanine Card (FMC) Standard (ANSI VITA 57.1)
  - Mezzanine/Carrier approach. Approx. 69 mm x 84 mm mezzanine size
  - Allows designing functionality once on a mezzanine so that it can be re-used on several carriers
  - Uses either a 160 pin (Low Pin Count) or a 400-pin (High Pin Count) connector
  - Most signals are freely definable and supposed to connect directly to an FPGA
  - Options possible: check for compatibility between Mezzanine and Carrier (Vadj, LPC/HPC, clocks)

Wishbone FPGA on-chip bus standard

- Wishbone , Rev B.4 Specification, OpenCores
  - Connects IP cores to each other inside an FPGA
  - Simple to use: point-to-point, data uni-directional
  - Easy to implement multi-point using crossbar switch design
  - Open standard with many cores available



Wishbone signals

Open Hardware Repository & CERN Open Hardware Licence

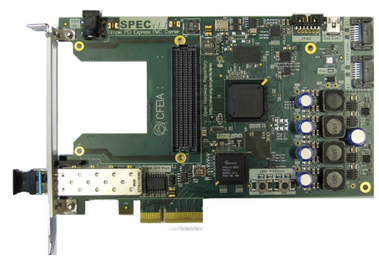
The Open Hardware Repository (OHR) at *http://ohwr.org* is a collaborative tool to share design information. A simple website is not enough. The OHR is developed using Chiliproject, an open source tool. It contains modules for Wiki pages, a File repository, News, Issue tracking and others.

Even for Open Hardware it is necessary to have a licence that defines the conditions under which a licensee will be able to use or modify the licenced material. It appeared that there was no existing licence usable to cover hardware developments. For this reason the Knowledge Transfer Group developed the CERN Open Hardware Licence (CERN OHL). In the spirit of knowledge sharing and dissemination, the CERN OHL governs the use, copying, modification and distribution of hardware design documentation, and the manufacture and distribution of products.

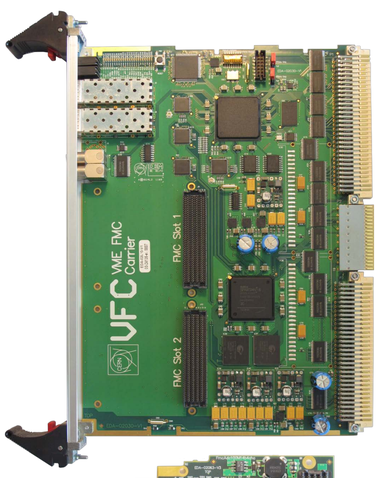
The CERN OHL shares the same principles as open-source software: anyone should be able to see the source (the design documentation in case of hardware), study it, modify it and share it. If modifications are made and distributed, it must be under the same licence conditions – this is the 'persistent' nature of the licence – which ensure that the whole community will continue benefiting from improvements.

Although the CERN Open Hardware Licence was originally written for CERN designs hosted in the Open Hardware Repository, it is also used by other designers wishing to share design information.

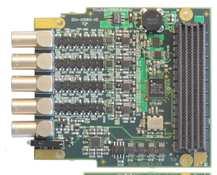
Designs in the Open Hardware Repository



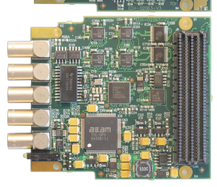
Simple PCIe FMC carrier – SPEC (produced by industry)
- One LPC (Low Pin Count) FMC slot
- One Spartan6 FPGA XC6SLX45T using Wishbone cores
- 2 Gbit DDR3 memory
- One Small Formfactor Pluggable (SFP) connector for White Rabbit
- Firmware loadable via PCIe



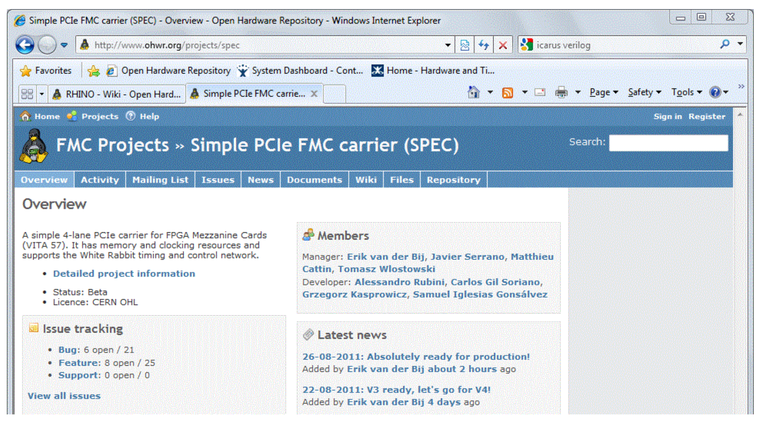
VME FMC Carrier – VFC (prototype available)
- VME64x with connectivity to Rear Transition Module
- Two LPC (Low Pin Count) FMC slots
- Two Spartan6 FPGA using Wishbone cores
- Two PLLs for clock cleaning and redistributing clocks
- On-board memory: two 72Mbit ZBT SRAMS, 2Gbit DDR3
- Two Small Formfactor Pluggable (SFP) connectors



FMC ADC 100M 14b 4ch – ADC (produced by industry)
- Four channel Analog to Digital converter
- 100 MSPS, 14 bits (ENOB 11.7 – 11 bit, SNR 72.2 - 67.7 dB)
- ±5V, 500mV, 50mV input range. Offset ±5V for each input range.



FMC DEL 1ns 4ch - Fine delay module (prototype available)
- Four channel output fine delay module
- 1 ns resolution or better
- 500 ns - 120 s range



Example of a project in the Open Hardware Repository

- Examples of other designs in OHR
  - nanoFIP: WorldFIP industrial fieldbus interface chip
  - Time-to-Digital Converter FMC with better than 1 ns resolution
  - White Rabbit timing network switch and firmware
  - ARM-based computer running Linux
  - TTL to NIM level converter in VME64x
  - Reconfigurable hardware interface for computing and radio (University of Cape Town, South-Africa)
  - Trigger/Timing logic Unit (Bristol University, UK)
- Examples of IP cores using Wishbone in OHR
  - VME64x core
  - Gennum PCIe bridge interface
  - DDR3 controller
  - Time to Digital Converter
  - Wishbone serialiser

Conclusions

- CERN needs to support its controls electronics for ten years or longer.
- Commercial-off-the-shelf electronics are usually black boxes supported by a single company.
- Developing Open Hardware allows designs according to our needs, with peer reviews and external help.
- Open Hardware can be produced and supported by any company, removing this burden from CERN.
- The CERN Open Hardware Licence (CERN OHL) provides a solid legal basis.
- The CERN OHL is also used for non-CERN designs.
- The Open Hardware Repository http://ohwr.org is a great environment to develop and document designs.
- OHR hosts over 45 active designs, also those outside CERN. Please ask if you want to host your next design.
- Most designs on OHR use standards (VME64x, PCIe, FMC, Wishbone) that stimulate re-use.
- Industry helps in developing Open Hardware and is producing and supporting Open Hardware.

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