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The Data Handling Processor (DHP) for the DEPFET Pixel Vertex Detector at BelleII

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A major upgrade of the current Japanese B-Factory (KEK-B) is planned by the fall of 2013. Together with this new machine (SuperKEK-B), also a new detector, BelleII, will be operated to fully exploit the higher luminosity (40 times larger than the previous experiment). One of the major changes in the new experiment will be the introduction of a new sub-detector, close to the interaction point, to allow a precise reconstruction of the decay vertices of the B meson systems. This pixel detector, based on the DEPFET technology, will consist of 20 ladder modules arranged in two cylindrical layers around the beam pipe. Each of the modules will be read-out independently by a combination of analog and digital ASICs placed at both ends of each sensor. The digital chip, the Data Handling Processor (DHP), is designed to control the readout chain and to pre-process and compress the data. The chip structure and the latest results will be presented.

Summary 500 words

The silicon pixel detector (PXD) developed by the international DEPFET collaboration consists of 20 DEPFET modules being readout independently (though synchronously) by the ASICs chips directly bump bonded on each module. Sensors are read-out row-wise with a frame rate of 50kHz. After digitization, the total raw data rate will be around 80Gbps/half module. To cope with these data rates a zero suppression is necessary. The Data Handling Processor chip (DHP) implements the zero-supression and dedicated data processing algorithm to correct for pedestal and common-mode offsets. Futhermore it synchronizes and controls switchers and drain current digitizer (DCD) chips.

All the raw data is being continuously stored into the chip memory. To optimize the chip efficiency, DHP chip processes that data only if the trigger signal is received. Upon the trigger arrival, the processing of the previously stored data starts, hits are recognized and sent to the chip output.

The chip is being implemented using the 90nm technology. In this talk conceptual solutions and latest results from the first test chip will be presented.

Author: Mr LEMARENKO, Mikhail (Physikalisches Institut-Universitaet Bonn)

Co-authors: Dr KRUEGER, Hans (Physikalisches Institut-Universitaet Bonn); Mr TEMPEREK, Tomasz (Physikalisches Institut-Universitaet Bonn)

Presenter: Mr LEMARENKO, Mikhail (Physikalisches Institut-Universitaet Bonn)

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