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Low Noise Preamplifier ASIC for the PANDA - Experiment

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For the electromagnetic calorimeter of the PANDA - Experiment the ASIC –Design –Group of the GSI –Experiment –Electronics department developed an integrated preamplifier and shaper ASIC. The chip developed for spectroscopy using is optimized for the readout of large area avalanche photo diodes (LAAPD) with a capacitance of 280 pF and an event rate of 350 kHz. Each ASIC has two equivalent analog channels consisting of a charge sensitive amplifier, a third order shaper stage and differential output drivers. The on chip implemented programmable voltage references are chosen to compensate the temperature dependancy on the output DC and ensure the full dynamic range.

Summary 500 words

PANDA (antiproton annihilation at Darmstadt) is a next generation hadron physics detector planned to be operated at the future facility for antiproton and ion research (FAIR) at Darmstadt, Germany. The subdetector for measuring photons, electrons and positrons is the electromagnetic calorimeter (EMC). It is built up of about 11000 lead tungstate crystals. Each crystal is read out by 2 large area avalanche photo diodes that have an active area of about 1 cmˆ2 and a detector capacitance of 280 pF. For the readout of these APDs an integrated preamplifier and shaper was developed in a 350 nm CMOS technology by GSI –Experiment - Electronics department.

The front –end amplifier is based on a single ended folded cascode circuit. The main focus during the development of the charge sensitive preamplifier was on the input stage. The free circuit parameters of the input stage had to be optimized for a large detector capacitance, the 350 kHz event rate and a low noise performance. Additionally there is a power consumption limitation due to the fact that the operation temperature will be T = -25℃.

The following first integrator stage is based on a downscaled version of the preamplifier circuit which fits well to the input potential. After the first integrator stage the signal path is splitted into two subpaths. One of these subpaths has an amplification of 32 in comparison to the other to get larger output signals in the low energy range which are less sensitive to interferences by pick up noise outside the ASIC. Each subpath is built up by two first order integrators. The second integrator provides a differential output signal.

A consequence of the high amplification in the analog chain is a high temperature dependency of the output DC voltages and a change of the amplifier operating points. The DC voltage dependency was measured to 25 mV/K. So with fixed voltage references a temperature shift would lead into a decreasing dynamic range of 2%/K. To solve this adjustable voltage references (three 10 Bit DACs) are implemented.

For monitoring purposes of the electronics a test pulser is implemented which permits a charge injection at the input of the preamplifier. A serial interface allows to write and read the DAC settings or trigger the test pulser. The on chip serial interface can be addressed by an individual 8 bit chip ID so a common bus structure of up to 255 ASICs can be realized. One address code is reserved for broadcast communication.

The characterization of the third ASIC iteration at a temperature of T = -25 ℃ and a detector capacitance of 280 pF results in an equivalent noise charge of ENC =(0.62 ± 0.03) fC and a maximum input charge of 6.3 pC. Therefore a dynamic range of over 10000 follows. The peaking time of the shaped signal was measured to t_p = (248 ± 3) ns. The event rate independent power consumption of one channel is P = (56.5 ± 0.5) mW.

The APFEL –ASIC fulfils all specifications required for the PANDA EMC. Especially the results for the equivalent noise charge are distinguished as well as the large dynamic range.

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