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Development of Low–Power Small–Area L–2L CMOS DACs for Multichannel Readout Systems

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The design and measurements of 8–bits DACs based on L–2L ladder architecture are presented. The main design goals were low power consumption and low area. Such features allow using the DAC for channel parameter trimming in multichannel readout system. The PMOS and NMOS based DACs are studied in wide range of biasing conditions and for two operation modes – as current generator and current divider. The prototypes of 0.034 mm^2 area are fabricated in 0.35μm CMOS technology. The measurements show that the maximum INL and DNL are both below 0.5 LSB. The power consumption is about 80μW.

Summary 500 words

In multichannel readout systems of high energy physics experiments the digital to analog converters (DACs) are commonly used to control various parameters like discriminator threshold voltages or current/voltage bias. In addition the systematic and random mismatches of CMOS technologies force the use of trimming DACs in order to obtain uniform channel behavior in multichannels ASICs. For these reasons a DAC with moderate (6 – 8 bits) resolution, low power consumptions and small die area is one of the basic building blocks requested in a multichannel readout system. \\

\indent The most popular DAC architectures like current steering or resistors ladder suffer from large number of elements which grows exponentially with increasing number of bits (2^{N} elements for N bits), what causes increasing layout complexity and area. The alternative architecture commonly used in old bipolar technologies is R–2R resistor ladder. This architecture needs only $4\mathrm{N}+1$ elements and may be attractive to design low area DAC circuits. However, modern CMOS technologies suffer from lack of high value resistors, and so using R–2R ladder architecture prevents to design low area low power DACs. Fortunately similar architecture can be successfully implemented using MOS transistors instead of resistors. In this work the two prototypes of 8 bit DACs implemented with both PMOS and NMOS transistors are presented.

The proposed DACs contains a MOS implementation of L–2L ladder and a low offset class AB OTA working as current to voltage converter.

Because of discontinuities of BSIM models the transistors of L-2L ladder (working in different regions from weak to strong inversion and from linear to saturation region) are not simulated correctly. For this reason the design methodology was based on phenomenological mismatch model.

The dimensions of NMOS transistors used in the ladder are $\mathrm{W/L} = 5\mu/25\mu$, while in the PMOS ladder are $\mathrm{W/L} = 7.5\mu/30\mu$. An important issue of L–2L DAC is to minimize the input offset of the OTA used as I–V converter. To obtain 8–bit resolution the output OTA was designed with random offset value below 2 mV (1σ). \\

\indent The first prototypes were fabricated in two–poly four–metal $0.35\ \mu\mathrm{m}$ CMOS technology. The DACs were tested in two operation modes – as a current generators and a current dividers. For both modes the DACs were tested in wide range of ladder transistors gate-to-source voltages, drain-to-source voltages and power supply voltages. In addition in current divider mode the tests were done for currents in the range between 1.6 and 51.2 μA. For nominal DAC settings – output current $\approx$ 6.4 μA, what corresponds to 25 nA LSB current and 0.5 mV LSB voltage step – the fabricated DACs show good INL and DNL below 0.5 LSB. A good DAC performance is also maintained for lower power supply voltages down to 1.7 V. The DAC power consumption in default conditions is about $80\mu W$ comprising of $\approx 20\mu$W of L–2L ladder and $\approx 60\mu$W of class AB amplifier.

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