Efficient Signal Contitioning by an FIR Filter for Analog Signal Transmission over Long Lines

Presented at the Topical Workshop on Electronics for Particle Physics 2011, 26-30 September 2011

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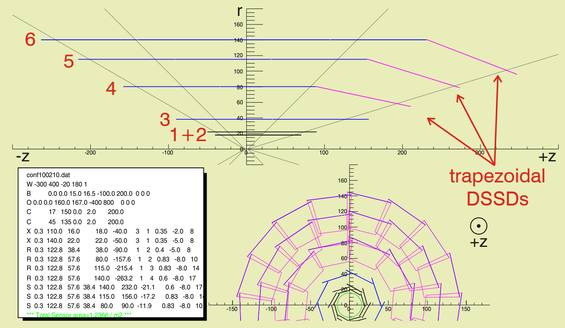
ABSTRACT

In the Belle II SVD readout chain the analog signals will be transmitted over long lines. This leads to signal distortion, caused by the frequency dependent transfer function of the cable and also by reflections, which occour whenever the line impedance changes.

One possibility to compensate these effects is a dedicated filter at the receiver end.
This poster describes the approach to realize the required filter as a finite impulse response (FIR) filter. We further show how such a filter can be implemented in the firmware of an FPGA and the required FIR coeffients can directly be calculated from the output signal of the APV25 front-end chip.

BELLE II SVD

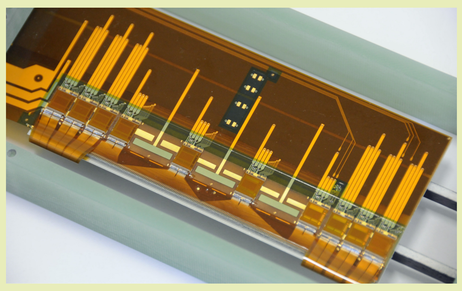
Layers: 4 strip (layers 3 to 6)
2 DEPFET pixels (layers 1 + 2)
Radii: 1.8 / 2.2 / 3.8 / 8 / 11.5 / 14 cm
Sensors: 187 rectangular double-sided silicon strip detectors (DSSD)
41 trapezoidal DSSDs for the slanted forward part
Active area: ~1.2 m^2, ~240 k strips
Front-end chip: APV25 (50 ns shaping time)
Shaping time: 50 ns
Cooling: CO_2 system (-20°C)



Belle II SVD layout (including 2 pixel layers)

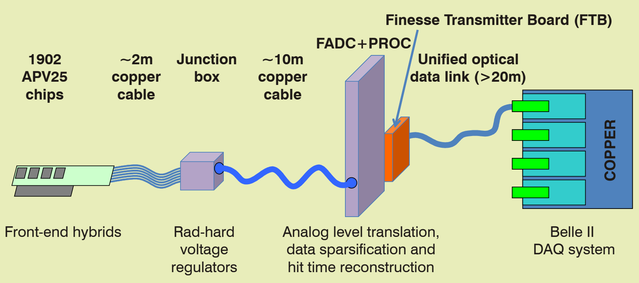
BELLE II SVD READOUT

Belle II Silicon Vertex Detector (SVD) Readout System

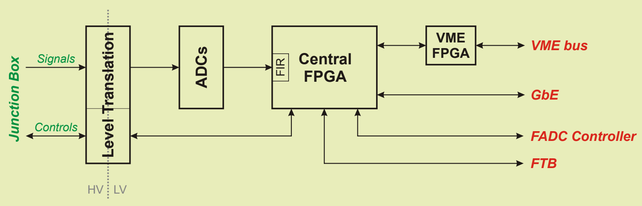


The Origami Module is the basic element of the Belle II SVD. It consists of a 6" double-sided silicon strip detector with the APV25 readout chips attached on one side. Pitch adapters made of flex circuits are bent around the edge to connect the strips of the bottom side – hence the name Origami. This concept allows a single, thin pipe running over all chips of a ladder for cooling with CO_2. The sensors are mounted on ribs which are a sandwich composite of carbon fiber sheets on an airex styrofoam core.

The differential outputs of the APV25 front-end are connected to a juction box outside the aceptance of the SVD. Apart from patch panels, the box contains radiation-hard voltage regulators to supply the front-end hybrids and protect them from transient over-voltages. On the far end, FADC+PROC modules will receive the analog data, digitize and analyze them. In total, the analog signals of the APV25 chips will be transfered over 12m long twisted pair copper cables.



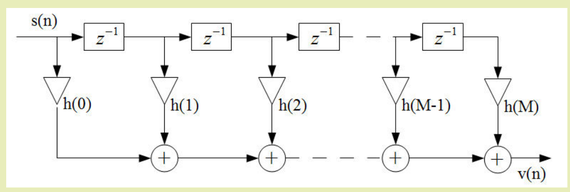
The FADC+PROC VME modules will perform analog level translation (from ±bias voltage down to ground) and digitization of the incoming data. The signals will be processed inside the central FPGA, an Altera Stratix IV GX. The first step is an FIR filter, followed by pedestal subtraction, common mode correction, sparsification and hit time finding.



FINITE RESPONSE FILTER IMPLEMENTATION

Finite Impulse Response (FIR) Filter

A finite impulse response (FIR) filter is a non-recursive digital filter that calculates the output signal as the weighted sum of a certain number of samples of the input signal. One possible realization (direct form) is shown in the picture below.



The number of filter coefficients M, which is equivalent to the number of used samples, is called the order of the filter.

An FIR filter has the following properties:

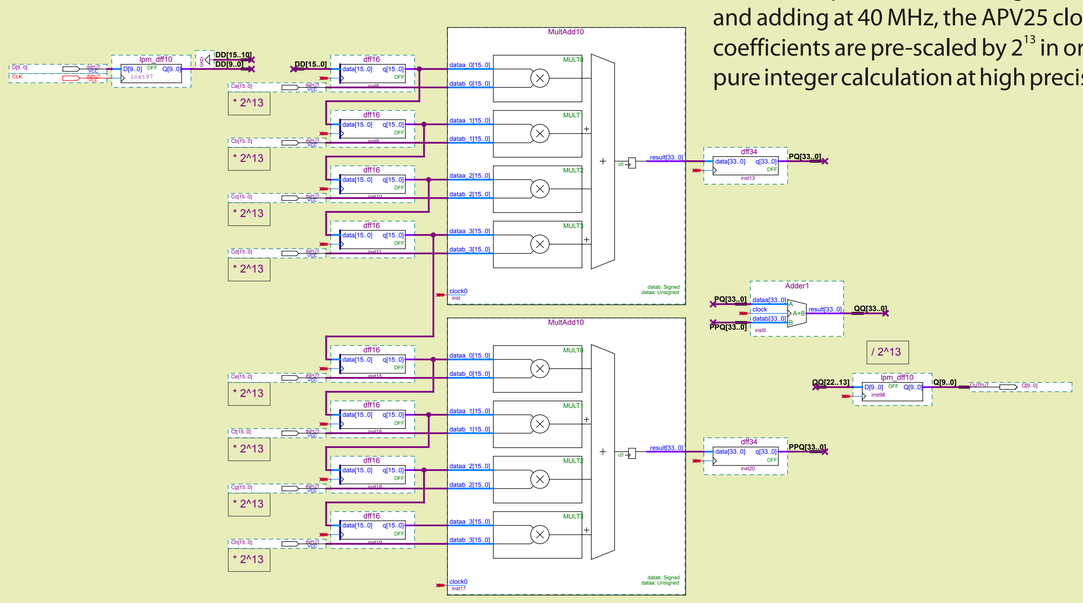
- limited number of coefficients
- linear time-invariant (LTI) system
- requires no feedback
- inherently stable

Obtaining FIR Filter Coecients

Determining the filter coefficients requires the impulse response of the system. Luckily, the APV25 delivers a single-clock tick mark once every 35 clocks when it is idle, which can be interpreted as the sampled impulse responses of the readout chain. For the calculation of the FIR filter coefficients, the tick marks are averaged over 300 events. Furthermore they are normalized so that the baseline is shifted to zero and the maximum value is set to one.

Implementation

For first tests, an FIR filter of the order 32 was implemented in software and verified. Then, the order was reduced to 8, which still yields excellent results. A filter with 8 coefficients has the advantage that it can be implemented in the firmware of the existing FPGAs (Altera Stratix 1) for each channel, and thus does not require additional hardware or space on the FADC boards. The Firmware implementation (see below) uses dedicated digital signal processor (DSP) blocks, which can perform 16 bit signed multiplication and adding at 40 MHz, the APV25 clock speed. The coefficients are pre-scaled by 2^{13} in order to enable pure integer calculation at high precision.

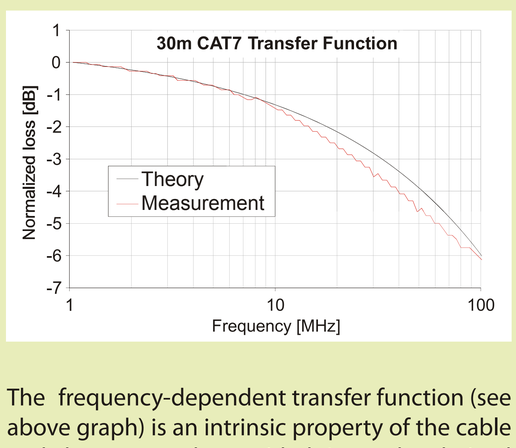


Schematics of the FPGA implementation; the used FPGA is an ALTERA Stratix 1 (EP1S20F672C7N)

THEORY

Cable Transfer Function

Every cable has a frequency-dependent transfer function, which causes distortion and widening of the original signal. Moreover, changes of the impedance along the line, in particular at every interconnection between cables and boards, lead to reflections. Even though the latter can be reduced by proper termination, this is never perfect in real life. In the end, both effects result in an unwanted additional contribution to the noise of the readout system.



The frequency-dependent transfer function (see above graph) is an intrinsic property of the cable and thus cannot be avoided. It can be derived from the telegraph equations as

$$H(f) = e^{-kl(1+j)\sqrt{f}} \qquad (1)$$

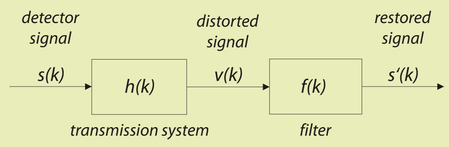
with

f .....frequency
k.....cable constant
l.....cable length

This transfer function can be compensated by a HF boost on the sender side ("pre-emphasis"), but also by an analog or digital filter ("equalizer") on the receiver side. As the APV25 chips are in the radiation zone, we cannot put any commercial electronics there, so we are confined to the receiving end.

Filter at the Receivers End

From the viewpoint of signal theory, the readout chain of the Belle II SVD can be described by the following figure



The diskrete signals *s(k)* and *v(k)* and the system impulse response *h(k)* are related by

$$v(n) = \sum_{k=-\infty}^{\infty} h(k)\, s(n-k) \qquad (2)$$

Our goal is to recover the initial signal, hence a filter *f(k)*, fulfilling the following relation, is required.

$$s'(n) = \sum_{k=-\infty}^{\infty} f(k)\, v(n-k) = s(n) \qquad (3)$$

Since we presume causality, it is required that *s(n-k) = 0* and *v(n-k) = 0* for *n < k*. For a practical implementation, *k* cannot become infinite and for easier handling we shift the sum to start at zero. So we obtain $0 \le k \le N$. The *f(k)* are then called filter coefficients of the filter system of the order *N + 1*. Then, equation *(2)* can expressed by matrices,

$$V_n = \sum_{k=0}^{N} H_{nk} S_k \quad or \quad \mathbf{V} = \mathbf{HS} \qquad (4)$$

with $H_{nk} = 0$ for $n<k$. The elements of the matrix **H** can easily be obtained from the pulse response of the system, where $s(n) = [1, 0, 0, \ldots]^T$:

$$\begin{bmatrix} h_0 & 0 & 0 & 0 & \cdots \\ h_1 & h_0 & 0 & 0 & \cdots \\ h_2 & h_1 & h_0 & 0 & \cdots \\ \vdots & \vdots & \vdots & \ddots & \cdots \\ h_N & \cdots & \cdots & \cdots & h_0 \end{bmatrix} \cdot \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ \vdots \end{bmatrix} = \begin{bmatrix} h_0 \\ h_1 \\ h_2 \\ \vdots \\ h_N \end{bmatrix} \qquad (5)$$

Once **H** is known, the original signal can be reconstructed by

$$\mathbf{S'} = \mathbf{H}^{-1}\mathbf{V} = \mathbf{FV} = \mathbf{H}^{-1}\mathbf{HS} \qquad (6)$$

where the filter matrix **F** can be identified as the inverse matrix of **H.** The first row of **F** contains the coefficients of the required filter.

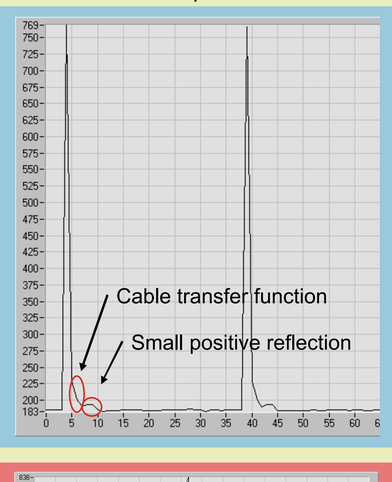
MEASUREMENTS

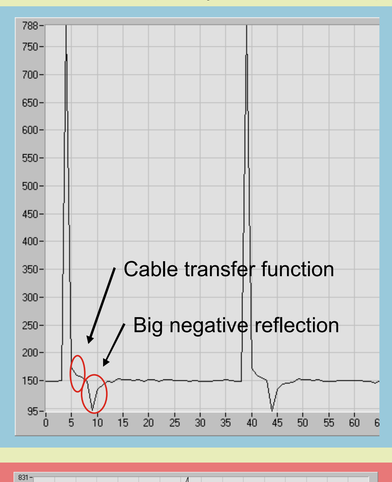
Comparison of APV25 signals with and without FIR filter

To evaluate the efficiency of the implemented FIR filter, two APV25 channels where measured with 12m long twisted pair cables between hybrid board and back-end electronics. While the cable termination was optimized for channel A, it was not for channel B. Hence, on channel B both negative effects, the signal distortion caused by the transfer function of the cable and huge reflections were observed without FIR filter. After implementation of an FIR filter with 8 coefficients, not only the frequency-dependent effects, but also the reflections, were completely removed.

Channel A (optimized termination) **Channel B** (non-optimized termination)

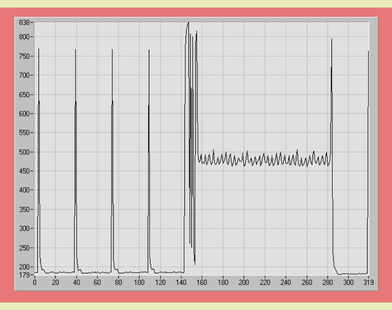
APV25 Tick Marks





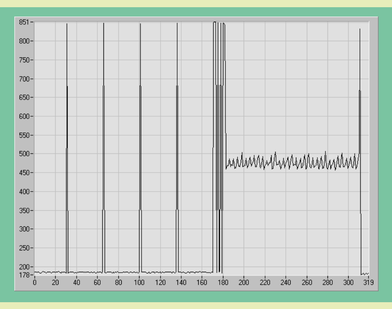
Luckily, the APV25 delivers single spikes ("tick marks") when idle, which can be interpreted as impulse response of the system. After averaging and normalization, the coefficients can be obtained by inversion of a triangular matrix.

Without FIR



The aftermath of the digital header causes significant noise in the first couple of analog signals in a data frame.

With FIR



The nasty effects are completely gone even for the non-optizimed channel and the digital header shows flat tops.

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