Contribution ID: **116** Type: **Poster**

Efficient Signal Contitioning by an FIR Filter for Analog Signal Transmission over Long Lines

Thursday, 29 September 2011 16:00 (2h 30m)

In the Belle II SVD readout chain the analog singnals will be transmitted over long lines. This leads to signal distortion, caused by the frequency dependent transfer function of the cable and also by reflections, which occour whenever the line impedance changes.
One possibility to compensate these effects is a dedicated filter at the receiver end.
This presentation describes the approach to realize the required filter as a finite impulse response (FIR) filter. We further show how such a filter can be implemented in the firmware of an FPGA and the required FIR coeffients can directly be calculated from the output signal of the APV25 front-end chip.

Summary 500 words

In the readout chain of the Belle II Silicon Vertex Detector, the differential outputs of the APV25 front-end chips will be connected to the Flash-ADC (FADC) boards by about 12m long twisted pair copper cables. Every cable has a frequency-dependent transfer function, which causes distortion and widening of the original signal. Moreover, changes of the impedance along the line, in particular at every interconnection between cables and boards, lead to reflections. Even though the latter can be reduced by proper termination, this is never perfect in real life. In the end, both effects result in an unwanted additional contribution to the noise of the readout system.

The frequency-dependent part can be compensated by a HF boost on the sender side (”pre-emphasis”) or a similar filter (”equalizer”) on the receiver side. As the APV25 chips are in the radiation zone, we cannot put any commercial electronics there, so we are confined to the receiving end.

In the first approach, a commercial analog equalizier chip (AD8128) was applied with moderate success. Even the filter can be adjusted over a wide range, resulting in a significant improvement of the signal shape, the distortion could not be compensated completely. A disadvantage of this chip is that it has a single-ended output and thus interrupts the otherwise fully differential design of the signal transmission.

Another possibility is to use a digital finite impulse response (FIR) filter, where the output is calculated as the weighted sum of a certain number of samples, equal to the filter degree. We will show how effiecent such a FIR filter can be used to deskew the signal of the APV25 chip attached to the FADC boards by a 12m long copper cable. The filter coefficients can easily be derived in situ from so-called tick marks (pulses) which are periodically issued by the APV25 in idle condition.

For first tests, an FIR filter of the order 32 was implemented in software and verified. Then, the order was reduced to 8, which still yields excellent results. A filter with 8 coefficients has the advantage that it can be implemented in the firmware of the existing FPGAs for each channel, and thus does not require additional hardware or space on the FADC boards. The Firmware implementation uses dedicated digital signal processor (DSP) blocks, which can perform 16 bit signed multiplication and adding at 40 MHz, the APV25 clock speed.

Measurements have shown that not only the frequency-dependent effects, but also the reflections, caused by imperfect termination, are completely removed by an FIR with 8 coefficients.

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Session Classification: Posters

Track Classification: Opto