First test results with the Gigabit Link Interface Board (GLIB)

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on behalf of the GLIB team
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Special thanks to Greg Iles
THE GLIB IS: an evaluation platform and an easy entry point for users of high speed optical links

THE GLIB IS TARGETED FOR:

- optical link evaluation in the laboratory
- control, triggering and data acquisition from remote modules in beam or irradiation tests
Introduction

GUIDELINES

✓ Rapid development
  ✓ Project approved in September 2010 -> first prototype targeted for spring 2011
  ✓ Reuse of existing hardware/firmware/software components
  ✓ Compatibility with commercial technologies

✓ Low cost
  ✓ Limit the FPGA logic resources & high-speed links
  ✓ Reuse of optical modules

✓ User-driven evolution potential
  ✓ Mezzanine cards
  ✓ FPGA pin compatible upgrades
  ✓ Firmware

✓ Long lifetime
  ✓ distribution and support of a small set of variants over several years
Double width AMC module (for stand-alone or μTCA crate environment).

Virtex-6 VLX130 (mid capacity but upgradeable up to VLX365) with 5Gbps/6.5Gbps transceivers.
Hardware

ARCHITECTURE (1/2)

JTAG
IPMI

Port [0:1]
Port [4:7]
Port [8:11]

Port [2:3]
Port [12:15]
Port [17:20]

FMC#1
JTAG
I/O
\textsuperscript{i}C
TRx
CLK

FMC#2
JTAG
\textsuperscript{i}C
I/O
CLK

\\textsuperscript{4}x SFP+

\textbf{CAPABILITY FOR VARIOUS PROTOCOLS (PCIe 4x, SRIO, XAUI)}

\textbf{FPGA}

Module Management Controller (MMC)

\textbf{MGT quad}

\textbf{Clock Distribution Circuitry}

\textbf{AMC edge connector}

\textbf{μTCA REDUNDANCY CAPABILITY}

\textbf{COMPATIBILITY WITH AMC13}

E. Hazen's Talk
Hardware

ARCHITECTURE (2/2)

- MGT Quad 116 (FMC#1)
  - REFCLK0
  - REFCLK1

- MGT Quad 115 (AMC port [4:7])
  - REFCLK0
  - REFCLK1

- MGT Quad 114 (AMC port [0:1])
  - REFCLK1

- MGT Quad 113 (AMC port [8:11])
  - REFCLK0
  - REFCLK1

- MGT Quad 112 (SFP+)
  - REFCLK1
  - REFCLK0

- Global Clock #1
- Global Clock #2
- Global Clock #3
- Global Clock #4
- Clockout #1
- Clockout #2
- Global Clock #5
- Clockout #3
- Global Clock #4
- Global Clock #5
- Clockout #6
- Clockout #7
- Global Clock #8

- Clock Distribution Circuitry
- Clock Multiplier & Jitter Attenuator
- PCIe clock jitter attenuator

- 40.079MHz 5mm x 7mm
- FPGA

- CLK2/TCLKB
- CLK1/TCLKA
- CLK3/FCLKA

- AMC edge connector

- Crystal oscillator
- Jumper

- FMC#1
- CLK1_C2M
- CLK0_C2M
- CLK1_M2C
- CLK0_M2C

- CLK#2
- CLK0_M2C
- CLK1_M2C
- CLK0_C2M
- CLK1_C2M

- SMA
Optical Control/Readout of FE modules w/ GBT (through SFP+)
Optical TTC reception (through TTC FMC)
PC w/ 1Gb Ethernet + Power supply

- GbE: GBT payload $\leftrightarrow$
  GLIB config $\leftrightarrow$

- GBT: Slow CTRL $\leftrightarrow$
  DAQ $\leftrightarrow$
  Timing/Trig $\leftrightarrow$

- Power Supply

- FPGA

- SRAM

- 3.2Gbps/link

- 144Mb

- Timing/Trig to FE

- GBT(s) FRONT-END

= TTC FMC  = SFP+
Introduction

TYPICAL USE CASES (2/3)

BENCH-TOP: front-end module test setup

- Electrical Control/Readout of FE modules w/ out GBT (through FE module i/f FMC)
- Optical TTC Reception (through TTC FMC)
- PC w/ 1Gb Ethernet + Power supply

**GbE:**
- GBT payload
- GLIB config

**E-Link:**
- Slow CTRL
- DAQ
- Timing/Trig

**Power Supply**

**FPGA**

**SRAM**

**GLIB**

**FRONT-END**

**144Mb**

**Up to 22 E-Links**

**80Mbps**

**160Mbps**

**320Mbps**

{Per E-Link}

**Timing/Trig to FE**

**BENCH-TOP:** front-end module test setup

= E-LINK FMC

= TTC FMC

= SFP+
Introduction

TYPICAL USE CASES (3/3)

CRATE: system test setup

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GBT: Slow CTRL DAQ Timing/Trig

PCIe: GLIB config GBT payload

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GBT(s) FRONT-END

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GBE switch PCIe switch Clock Distr.

MCH μP

Commercial MCH

GLIB

FPGA

CPU

Storage

Crate Management

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Timing/Trig to FE

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TYPICAL USE CASES (3/3)

CRATE: system test setup

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2011.09.29
Hardware

GLIB V.1 (PROTOTYPE) – top view
Hardware

GLIB V.1 – bottom view
Hardware

GLIB v.2 (PREPRODUCTION)

MMC mezzanine card v3

V. Bobillier's Talk

All knows issues resolved
Firmware

TOP LEVEL

Use of GBT FPGA firmware IP  
(by Sophie Baron, Steffen Muschter et al)

IPBUS firmware IP  
(by Dave Newbold et al)

G. Iles's Talk
Achievements

✓ All high-speed links operating without problems at up to 5Gbps
  (maximum data rate with the current speed grade of the FPGA)
✓ Interface with a PC through the 1Gb Ethernet PHY (UDP)
✓ Successful IPMI communication with MCH in a uTCA crate
✓ Integration of 8 GBT links in the FPGA in less than 50% of the FPGA logic resources
  (without applying any GBT-FPGA resource optimization techniques)
✓ Reception of data sent by a GBT chip at 4.8Gbps
✓ GBT protocol communication between two non-synchronized GLIB cards
  (the “BE” GLIB receiving TTC clock from external source,
  the “FE” GLIB recovering the TTC clock from the data stream sent by the “BE” GLIB, see next slide)
Achievements
Achievements
Two different setups are available.

The setups include:

- Crate
- MCH
- Power supply
- CPU
- Commercial cards

The TCA infrastructure study became a different project “xTCA Evaluation Project” led by M. Joos.

M.JOOS talk
Software

JAVA GRAPHICAL USER INTERFACE

- Use of IPbus software (by Robert Frazier et al)
  G. Iles's Talk

- Stand alone JAVA GUI under development
Mezzanine cards

TTC FMC ARCHITECTURE

- CDR for rates between 10Mb to 675Mbps
- Compatible with HPC & LPC FMC sockets
- Compatible with 2.5V FMC carriers (e.g. Virtex-6 based)
- Based on TTC reception circuitry & firmware of AMC13

E. Hazen's Talk

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TTC FMC in beam test setup
Mezzanine cards

**TTC FMC IMPLEMENTATION**

First tests with a TTCvi show good results

- Successful 40MHz clock recovery (with deterministic phase)
- Successful decoding of A & B channel (Level 1 Accept & Broadcast commands)
SUMMARY & OUTLOOK

✓ 2pcs of GLIB v1 manufactured in Q1 2011, most of functionality ok, only few issues found.

✓ All issues understood and solved in GLIB v2. 2pcs manufactured in Q3 2011. No issues found yet.

✓ Preproduction of another 4pcs of GLIB v2 ongoing. Delivery to beta users in Mid November 2011
  FPGA with higher speed grade will be used (for 6.5Gbps transceivers)
  Associated firmware, software and TTC FMC mezzanines will also be delivered.

✓ Production version expected to be available by July 2012.
  Need to define the quantity to order. If interested, please contact us by April 2012.

✓ xTCA firmware development will start in January 2012 (xTCA infrastructure available)

✓ Software development ongoing

✓ Auxiliary cards under developmentfirst prototypes by Q1 2012.
  TTC FMC prototype already available (2pcs + 2pcs by mid November 2011)
  Versatile Link FMC, PCI Express adapter, Digital IO FMC prototypes available by Q1 2012
GLIB website

GLIB Specifications document

GLIB schematics

GLIB at Open Hardware Repository

Contact