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First test results with the Gigabit Link Interface Board (GLIB)

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We have designed and built an FPGA-based platform for users of high speed optical links in high energy physics experiments. The Gigabit Link Interface Board (GLIB) serves both as a platform for the evaluation of optical links in the laboratory as well as a triggering and/or data acquisition system in beam or irradiation tests of detector modules. The GLIB is a double width Advanced Mezzanine Card (AMC) that is used either stand-alone or inside a μTCA crate. This paper presents test results with the first GLIB prototypes delivered in January 2011 and reports on a setup demonstrating its use in a GBT-based system.

Summary 500 words

We have designed and built an FPGA-based platform for users of high speed optical links in high energy physics experiments. The Gigabit Link Interface Board serves both as a platform for the evaluation of optical links in the laboratory as well as a triggering and/or data acquisition system in beam or irradiation tests of detector modules.

The GLIB is a double width Advanced Mezzanine Card that can be used either stand-alone or in a μTCA crate. Each GLIB hosts four sockets for SFP+ transceiver modules connected to Virtex-6 FPGA transceivers operating at up to 6.5Gbps. This performance matches comfortably the specifications of the GBT/Versatile Link project with its targeted data rate of 4.8Gbps. In its simplest form, one GLIB board thus interfaces with up to four GBT channels. When in a μTCA environment, the GLIB communicates with the outside world through the standard Gigabit Ethernet endpoint and is interconnected with other cards in the shelf, depending on the backplane configuration, through a PCI Express x4 GEN2 compatible link. When in stand-alone operation, the system interfaces with a PC through a Gigabit Ethernet RJ45 socket and/or a PCIe x4 GEN2 adapter board. Special design considerations have been applied in order to ensure maximum flexibility and ease of upgrade. The GLIB includes two FPGA Mezzanine Card (FMC) sockets for enhancing its I/O capability. Each FMC socket provides up to 160 user-specific I/Os (that can be configured both as single-ended or differential pairs) as well as 2 differential clock inputs and 2 differential clock outputs. One of the two FMC sockets also offers four optional 6.5Gbps transceiver lines. This gives users the flexibility to adapt the GLIB interface to their system, by for instance adding connectivity to the TTC network at the back-end, or connecting to e-links at the front-end. Additionally, the flexible clock distribution circuit based on cross-point switches and clock synthesizers allows the use of various clock sources and numerous implementations of high speed serial link protocols. Finally, there is the possibility to use pin-to-pin compatible FPGAs with higher density and/or speed grade.

This paper presents test results with the first GLIB prototypes delivered in January 2011 and reports on a setup demonstrating its use in a GBT-based system. The setup consists of two stand-alone GLIB boards that are interconnected with optical links. The two GLIBs interface with a PC through Gigabit Ethernet. The first GLIB emulates a GBT chipset connected to front-end modules while the second one plays the role of the back-end system that delivers clock, fast and slow commands and reads out front-end data. Additionally, we envisage the use of an FMC mezzanine that adds connectivity to the TTC network at the back-end.

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