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TEL62: an integrated trigger and data acquisition board

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The main goal of the NA62 experiment at the CERN SPS is to measure the branching ratio of the K+ ⟶ π+νν decay, collecting about 100 events in two years of data taking.
The nature of the experiment puts stringent requirements on the trigger and data acquisition system: the efficient online selection of interesting events and loss-less readout at high rate will be key issues. Readout uniformity among different sub-detectors and scalability were taken into account in the architecture design. For this purpose an integrated trigger and data acquisition board (TEL62) has been designed and the first prototype is currently under test.

Summary 500 words

Introduction

The NA62 experiment at the CERN SPS aims at measuring the ultra-rare kaon decay K+ ⟶ π+νν as a highly sensitive test of the Standard Model (SM) and a search for New Physics. Experimentally, the detection of this process is very difficult due to the smallness of the signal and the presence of a very sizeable concurrent background, so a very low undetected DAQ inefficiency, below 10−8 is an important issue.
Efficient online selection of candidate events represents a very important issue for this experiment, because of the large reduction to be applied before tape recording. A common general-purpose integrated trigger and data acquisition board (TEL62) has been designed. The Trigger and Data AcQuisition (TDAQ) system architecture and the TEL62 board architecture and design solution are described in the follow.

TDAQ architecture

The rate of events in the decay region is strongly dominated by background. The rate on main detectors is around 10MHz. An additional rate of about ˜1MHz of muons coming from the beam production target must also be taken into account. The single hardware L0 trigger is used to reduce the total rate to ˜1MHz using information coming from the RICH, Large Angle Veto (LAV), Liquid Krypton (LKr) calorimeter and Muon Veto (MUV) detectors. The trigger primitives from each detector involved in L0 trigger decisions will be built in the same board used for digitization and monitoring. For almost all sub-detectors in NA62 the building block of this system will be the TEL62 board.
The TEL62 board

The TEL62 board is a major upgrade of the TELL1 board designed by EPFL Lausanne for the LHCb experiment at CERN. The design exhinits a similar overall architecture, but the board is based on much more powerful and modern devices, resulting in more than 4 times the computational power and more than 20 times the buffer memory of the original, plus several other improvements in terms of connectivity. The on-board logic is hosted by 5 large FPGAs of type Altera EP3SL110, connected in a star topology.
In details:
1. 4 FPGAs (“PP”) are each connected to mezzanine cards (in particular newly designed TDC boards for NA62) through a 200 pins connector, and also to 2-GByte DDR2 memory buffers (SODimm form factor). The data received from the mezzanine cards is both stored in the memory and processed on the fly to generate L0 trigger primitives.
2. The central FPGA (“SL”) receives the L0 primitives from individual “PPs”, merges them and sends them to another custom mezzanine, “Quad-GbE”, which implements 4 x 1Gbit Ethernet channels used to connect the TEL62 boards to the Level0 central processor, and possibly to other TEL62 boards in a daisy-chain configuration. The Level0 processor elaborates and matches trigger primitives from all sub-detectors, leading to a L0 trigger accept/reject for each event. If an event is accepted all readout boards are informed through a TTC optical link, the relevant data is extracted from the on-board memory buffers and transmitted to the DAQ through other Ethernet links on the “Quad-GbE”.
3. The slow control and configuration of the board is handled by an on-board credit-card PC (CCPC) running Linux.
4. The clock of the system and the L0 trigger information are distributed to all the TEL62 boards through a

CERN-standard optical TTC link. The TEL62 uses a TTC receiver chip (TTCRx) to decode clock and trigger information.
The board size follows the 9U Eurocard standard. The printed circuit is made of 16 layers, with all lines controlled in impedance (50 ohm). Special care has been used to route the clock tree, to avoid as much as possible signal jitter. In total a production of 80 boards plus spares is foreseen for NA62.
Currently the first prototype is under test; a first pre-production is foreseen in the next months and the final production in 2012.

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