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FF-EMU: a radiation tolerant ASIC for the distribution of timing, trigger and control signals in the CMS End-Cap Muon detector

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A radiation tolerant integrated circuit for the distribution of clock, trigger and controls in the Front-End electronics of the CMS End-Cap Muon detector has been developed in the IBM CMOS 130nm technology. The circuit houses transmitter and receiver interfaces to serial links implementing the FF-LYNX protocol that allows the integrated transmission of triggers and data frames with different latency constraints. Command encoder and decoder modules associate transitions in trigger and control signals to data frames. The circuit architecture and results of test and characterization of the prototypes will be presented.

Summary 500 words

Copper cables for the control and readout of the Front-End electronics in the ME1/1 station of the CMS End-Cap Muon detector will be replaced with optical links during the first scheduled LHC shutdown. This will increase the overall performance of the readout system, currently limited by the reliability of long (~15m) high-speed (280Mbps) electrical links. In addiction more space will be available for connections to the new Front-End boards whose insertion is foreseen (from 5 to 7 boards in each detector chamber). The FF-LYNX protocol has been selected for the integrated distribution of Timing, Trigger and Control (TTC) signals because of its flexibility (e.g.: different speed options), radiation tolerance of critical information (e.g.: trigger timing, frame size) and compatibility with different latency requirements (e.g.: fixed and short latency for time-critical information, as triggers and calibration pulses, unbounded latency for other control and monitoring signals). Transmitter (TX) and Receiver (RX) interfaces to double-wire (i.e.: separate lines for clock and data) serial electrical links were already available as radiation tolerant IP-cores for ASIC and FPGA developments. Existing interfaces (320 Mbps) have been customized with the introduction of a DC balanced encoding in data frames to make them compatible with optical links. The reference clock is recovered with the proper phase in the RX interface from the 320 MHz incoming clock and transmitted to the Front-End electronics. Command encoder and decoder modules have been developed to associate transitions of trigger, control and monitoring signals to FF-LYNX frames. A token-based watchdog mechanism is used to monitor rare radiation induced effects not handled by the internal redundancy of the protocol and of the interfaces and trigger the required reset procedure. An embedded I2C interface is used to read error counters that monitor Single Event Upset events. An FPGA based test-bed including a custom printed circuit for irradiation tests and a PCI-Express "off-the-shelf" board (PLDA XpressV6) for test pattern generation and output data monitoring has been developed, as well as a custom card (EMU_CC) that will let to interface new Front-End (DCFEB) and Back-End (O-DMB) boards with existing hardware (CFEB and DMB). The prototype of the FF-EMU circuit, developed in the IBM CMOS 130nm technology, has been submitted for fabrication in February 2011. Results of test and characterization of the prototypes will be presented as well as a detailed description of the architecture and behavior of the FF-EMU circuit and of the entire detector control system.

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