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A PowerPC-based control system for the ReadOut Driver module of the ATLAS IBL.

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he ATLAS experiment at LHC planned to upgrade the existing Pixel Detector with the insertion of an innermost silicon layer, called Insertable B-layer (IBL).A new front-end ASIC has been foreseen (named FE-I4) and it will be readout with improved off-detector electronics. In particular, the new Read-Out Driver module (ROD) is a VME-based board designed to process a four-fold data throughput. Moreover, the ROD hosts the electronics devoted to control operations whose main tasks are: providing setup busses to access configuration registers on several FPGAs, receiving configuration data from external PC, managing triggers and running calibration procedures. In parallel with a back-compatible solution with a DSP, a new ROD control circuitry with a PowerPC embedded into a FPGA has been implemented. In this paper the status of the PowerPC-based control system will be outlined, with major focus on firmware and software development strategies

Summary 500 words

The first upgrade foreseen at the ATLAS experiment at LHC will be the insertion of an innermost silicon layer, called Insertable B-layer (IBL). A new front-end ASIC has been designed (named FE-I4). To readout this new pixel layer an update of the readout electronics is necessary and it will be realized with two VME-based boards:
the Back Of Crate module (BOC) implementing optical I/O functionality and the ReadOut Driver
module (ROD) implementing data processing functionality. The ROD hosts the electronics devoted to control operations whose main tasks are: providing setup busses to access configuration registers on several FPGAs, receiving configuration data from external PC, managing triggers and running calibration procedures. In parallel with a back-compatible solution with a DSP, a new ROD control circuitry with a PowerPC embedded into a FPGA has been implemented. Development strategies and status of the activities in implementing a PowerPC based system are presented. Major focus will be on the firmware and software design. In particular several solutions will be described: connection methodology with the Atlas control system, implementation of custom logic and its integration with the embedded processor and strategies toward a combined software-firmware simulation environment.

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