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# Use of FPGA embedded processors for high performance data compression

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We present test results and characterization of a data compression system for the readout of the NA62 liquid krypton calorimeter trigger processor.
The Level 0 electromagnetic calorimeter trigger processor of the NA62 experiment at CERN receives digitized data from the calorimeter main readout board. These data are stored on-board on DDR2 latency memories and readout upon reception of a Level 0 accept signal.
The maximum raw data throughput at the output of the trigger front end cards is 2.6 Gbps.
To readout these data over two Gigabit ethernet interfaces we implemented two data compression systems: one based on a simple hard wired zero suppression algorithm implemented in the FPGA and one based on an FPGA embedded processor running a flexible data compression C code.
The two algorithms are tested on simulated Monte-Carlo events and compared with respect to maximum achievable readout bandwidth, maximum compression ratio and impact on readout latency.

## Summary 500 words

High performance data compression plays a central role in many areas of science and technology ranging from trigger and data acquisition systems for high energy physics experiments to high performance parallel scientific computing. We present test results and characterization of a high performance data compression system based on a last generation FPGA and an embedded processor.
The first FPGA embedded processors were introduced at the beginning of 2000. After ten years FPGA embedded processor technology has become mature, reliable and widely diffused.
We implemented an FPGA embedded processor data compression system for the readout of the NA62 liquid krypton electromagnetic calorimeter trigger processor.
The NA62 experiment at the CERN SPS aims to measure the Branching Ratio of the very rare kaon decay K+ -> pi+ nu nubar collecting ˜100 events with a 10% background in two years of data taking. One of the main background to the proposed measurement is represented by the K+ -> pi+ pi0 decay. To suppress this background an efficient photo veto system is foreseen. The NA48 liquid krypton high-performance electromagnetic calorimeter is used in the 1-10 mrad angular region.
The Level 0 electromagnetic calorimeter trigger identifies electromagnetic clusters in the liquid krypton calorimeter and sends to the Level 0 central trigger processor a time-ordered list of reconstructed clusters together with the arrival time, position, and energy measurements of each cluster.
Each front end board of the Level 0 electromagnetic trigger processor receives 16 bits words of digitized data from 32 electromagnetic calorimeter trigger tiles at a frequency of 40 MHz. These data are stored on-board on DDR2 latency memories and readout after 100 us upon reception of a Level 0 accept signal.
Given the maximum allowed L0 readout rate of 1 MHz the total raw data throughput at the output of the Level 0 trigger front end cards is 16 bit x 5 samples x 32 tiles x 1 MHz = 2.56 Gbps. These data are readout by a trigger and readout mezzanine mounting an Altera Stratix II FPGA with two Gigabit ethernet interfaces.
To readout all these data over two Gigabit ethernet interfaces we implemented two data compression systems. The first data compression system is based on a simple hard wired zero suppression algorithm implemented in the FPGA. The second one is based on a Nios II Altera processor running a flexible data compression C code. The two algorithms are tested on simulated Monte-Carlo data and compared with respect to maximum achievable readout bandwidth, maximum compression ratio and impact on readout latency.

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