Semiconductor Manufacturing in Austria

Topical Workshop on Electronics for Particle Physics
Vienna, Sept. 26th, 2011

Rainer Minixhofer – Senior Manager R&D
austriamicrosystems AG
Outline

Introduction, Company Overview and some History

High Voltage Technology

More than Silicon

3D IC Integration

Conclusions
Company milestones

1981  Austria Mikro Systeme (AMS) founded as joint venture by American Microsystems Inc. (AMI) and Voest Alpine (Austria)

1993  AMS goes public on Vienna exchange

2000  AMS returns to private status (major shareholder Permira Private Equity), becomes austriamicrosystems

2002  New 200 mm (8") fab goes on-line

2004  IPO on SIX Swiss Exchange in Zurich

2006  New test facility in Asia

2011  Acquisition of Texas Advanced Optoelectronic Solutions (TAOS)

⇒  A leader in high performance analog ICs: 1,100+ employees, 6 design centers, 19 offices worldwide
Full supply chain under one roof
Full Service Foundry

Your one-stop-shop for turn-key high performance analog IC solutions

**Specialty Processes**
- 180nm, 350nm, 800nm
- CMOS, High-Voltage, SiGe, NVM
- Automotive and medical certified
- Zero defect program
- Extended temperature range
- Second source capabilities

**Foundry Services**
- MPW service with cooperation partners
- Benchmark design environment
- Numerous digital & analog IP-cells
- Standard package assembly service
- In-house mixed-signal test facility
- Qualification services

**More than Silicon®**
- Custom processes
- 3D IC using TSVs
- RGB & IR Color Coating
- Extended IP portfolio
- Consultancy: ESD, DFM, DFY, …
- Adv. packages: WLCSP, Bumping, …
austriamicrosystems at a glance

- Design and manufacture of high performance analog ICs
- Ultra-low power, high accuracy, high integration
- Power Management – Sensors & Sensor Interfaces – Mobile Infotainment
- Global customer base includes major OEMs
- Integrated manufacturer: world class design + best-in-class manufacturing
# Our business

## Core expertise
- **Power Management**
- **Sensors & Sensor Interfaces**
- **Mobile Infotainment**

## Target markets

<table>
<thead>
<tr>
<th>CONSUMER &amp; COMMUNICATIONS</th>
<th>INDUSTRY &amp; MEDICAL</th>
<th>AUTOMOTIVE</th>
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<tbody>
<tr>
<td>Power management</td>
<td>Sensors &amp; sensor interfaces</td>
<td>Sensors &amp; sensor interfaces</td>
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<tr>
<td>Lighting management</td>
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<td>Bus systems</td>
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<td>Mobile infotainment</td>
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<td>Wireless</td>
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- **33% of revenues 2010**
- **54% of revenues 2010**
- **13% of revenues 2010**
Corporate responsibility

Environment

- State-of-the-art abatement systems
- Continuous energy saving and CO₂ reduction measures
- Promoting FSC and MSC products

Stakeholder Responsibility

- Participation in UN Global Compact for good business practices
- Company Code of Conduct for stakeholder relations

Strategic goal to become CO₂ neutral as a company
Worldwide network – design, sales, distribution

- 6 design centers:
  Austria, Switzerland, 2x Italy, Spain, India
- 19 sales offices, over 30 distributors worldwide

Distribution partnerships strengthened
Global contracts with tier 1 players
Austria – famous for

- Red Bull
- Vienna Philharmonic Orchestra
- Swarovski Crystals
- New Year's Concert
But Graz was home of famous scientists too

Let’s start with Ernst Mach

“Did you see an atom personally?”
(Ernst Mach to his physics students in Vienna about 1900)
Moore's Law

1958 (TI)  
Invention of IC

1947 (Bell Labs)

2011:
Tri-Gate (Intel 22nm):
10 Million Trans./mm²
1 Billion on 100mm².
# Technology portfolio

<table>
<thead>
<tr>
<th>Technology</th>
<th>800nm</th>
<th>350nm</th>
<th>180nm</th>
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<tbody>
<tr>
<td><strong>CMOS</strong></td>
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<tr>
<td>• Mixed Signal CMOS</td>
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<tr>
<td>• High Perf. Analog</td>
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<td><strong>RF Technologies</strong></td>
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<tr>
<td>• RF CMOS</td>
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<tr>
<td>• BiCMOS (SiGe)</td>
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<td><strong>HV Technologies</strong></td>
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<td>• HV CMOS</td>
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<tr>
<td>• Galvanic Isolation</td>
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<tr>
<td><strong>Embedded NVM</strong></td>
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<tr>
<td>• Emb. EE / Flash</td>
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<td>⬤</td>
<td>⬤</td>
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<tr>
<td>• OTP (Fuse)</td>
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<tr>
<td><strong>3D integration</strong></td>
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<tr>
<td>• Through Silicon Via</td>
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<tr>
<td>• Backside RDL</td>
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<td><strong>Sensor technologies</strong></td>
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<tr>
<td>• Hall</td>
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<td>⬤</td>
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<tr>
<td>• Opto</td>
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<td>⬤</td>
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</tbody>
</table>

- ⬤ available
- ⬤ in dev.
- ⬤ intended

Rev. 3/2011
Rdson vs. BVdss for HVCMOS (blue closed symbols) and BCD (white open symbols).
AMS 180nm HVCMOS shows largest BVdss range and very low Rdson.
Application Areas of Power Devices

- Motor Control
- Power Converters/Power Supplies
- Lighting Ballast
- Telecommunication (e.g., SLIC)
- Display Electronics
- Automotive

- Systems is partitioned into control chip that drives a set of discrete power SC devices
- Hybrid integration

- Current (A)
  - 5V CMOS: 5, 10, 100, 1000
  - 20V: 5, 10, 100, 1000
  - 50V: 5, 10, 100, 1000
  - 120V: 5, 10, 100, 1000

- Operating Voltage (V)
  - 5V CMOS: 5, 10, 100, 1000
### Broad standard product portfolio

#### Power Management
- PMUs
- Lighting
- Supervisors & Comparators
- LDOs
- DC-DC Converters

#### Mobile Entertainment Systems
- Mobile Entertainment Players
- High Performance Microcontroller

#### Audio
- Audio Front-ends
- Amplifiers
- Phones (Feature/Basic)

#### Sensors & Sensor Interfaces
- Magnetic Rotary Encoder
- Magnetic Linear Position Encoder
- Automotive Rotary Encoder
- Metering

#### Interfaces
- Display and LED Drivers
- LVDS
- Industrial Bus
- FlexRay / Automotive Bus Systems

#### RF Products
- High Frequency
- Low Frequency
- 5-20V HV

#### Data Converters
- A/D Converters
- D/A Converters
- Digital Potentiometers
- Analog Switches
- Data Acquisition Front-ends

### Leader in low power and high accuracy for communications, industrial, medical and automotive applications
High flexibility through modularity:

- SiGe BiCMOS
- High Voltage
- Non-Volatile Memory
- High sensitivity opto-process

Caps: poly & MIM
5V transistors
LVT transistors
3rd and 4th metal
Hi-resistive polysilicon
Poly- & Zener-fuses

350nm 3.3V analog/mixed signal polycide process
350nm vs. 180nm HV transistor comparison: 20V PMOS

AMS 350nm HVCMOS

AMS/IBM 180nm HVCMOS

Additional 30% average HV area reduction by shrinking to 180nm
Process modularity of 180nm technology

High flexibility through modularity:

- High Voltage
- Non-Volatile Memory
- metal-metal caps
- 5V transistors
- up to 7 layers of metal
- power metal (Cu and/or Al)
- hi-resistive polysilicon
- OTP (eFuse)

180nm 1.8V silicide process
180nm CMOS-HV 20V & 50V

Full modularity with CMOS base process, low mask count

180nm CMOS + HVCMOS

Low-voltage CMOS

180nm HV = 180nm RFCMOS + 2 Mask Levels
(2 wells, no HV gate oxide)
Gate Module of 180nm technology

Only 180nm HV technology on the market with 3 gate oxides!
Suite of FETs with three gate oxide thicknesses

- Low Voltage (LV) fets for standard 1.8 and 5V CMOS
- LV fets in HV well for high voltage isolation to substrate
- HV asymmetric fets for High Voltage applications
- 3 gate oxide thicknesses, 2 maximum drain bias choices
- HV symmetric fets for specialty applications (transmission gate)

<table>
<thead>
<tr>
<th>Vgs</th>
<th>Vds</th>
<th>LV fets</th>
<th>LV fets in HV well</th>
<th>HV asymmetric fets in HV wells</th>
<th>HV symmetric fets (nfet in Substrate)</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>1.8V</td>
<td>5.0V</td>
<td>1.8V</td>
<td>5.0V</td>
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<td>20V**</td>
<td>50V</td>
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<td></td>
<td>20V</td>
<td>50V</td>
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<tr>
<td>1.8V (3.5nm)</td>
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<td>nfet*</td>
<td>nfet*</td>
<td>nfeti20t</td>
<td>nfeti50t</td>
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<tr>
<td></td>
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<td>pfet*</td>
<td>pfet20t</td>
<td>pfet50t</td>
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<td></td>
<td></td>
<td>nfethvt</td>
<td>nfetihvt</td>
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<tr>
<td>5.0V (12nm)</td>
<td>nfetm</td>
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<td>nfetim</td>
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<td>pfet20h</td>
<td>pfet50h</td>
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</tbody>
</table>

* RF layout available  ** 25V Vds for nfeti25m,pfeti25m
Floating Logic

Substrate Logic – 350 and 180nm

• CORELIB (260 Cells) built up with PMOS4 and NMOS4
• Bulk of NMOS always PSUB
• Bulk of PMOS maximum of 3.3V

Floating Logic - only in HVCMOS

• CORELIB_HV has to be built with PMOSI and NMOS4I
• Bulk of NMOS 0V .. 46.7V
• PMOS maximum of GNDF+3.3V (max. 50V)
• Automatically generated form CORELIB

Net +2 additional alignments
CORELIB vs. CORELIB_HV Cell Layout

CORELIB Cell

CORELIB_HV Cell

Same Cell Size

NTUB

DNTUB

SNTUB

DNTUB

PSUB

RPTUB = SPTUB + DPTUB
### 180nm HVCMOS metal stack options

<table>
<thead>
<tr>
<th># Levels</th>
<th>AM Last Metal Option</th>
</tr>
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<tbody>
<tr>
<td>3</td>
<td>MT</td>
</tr>
<tr>
<td>4</td>
<td>MT</td>
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<tr>
<td>5</td>
<td>MT</td>
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<tr>
<td>6</td>
<td>MT</td>
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<tr>
<td>7</td>
<td>MT</td>
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</table>

#### Standard Al wiring Levels

<table>
<thead>
<tr>
<th>AM (4µm)</th>
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<tbody>
<tr>
<td>MT</td>
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<tr>
<td>M3</td>
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<td>M3</td>
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<td>M3</td>
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<td>M3</td>
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</table>

#### RF/analog add on module

<table>
<thead>
<tr>
<th>MT</th>
<th>M3</th>
<th>M2</th>
<th>M1</th>
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<tbody>
<tr>
<td>M1</td>
<td>M1</td>
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</table>

#### Standard CMOS layers

<table>
<thead>
<tr>
<th>MT</th>
<th>M1</th>
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</thead>
<tbody>
<tr>
<td>M3</td>
<td>M2</td>
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</tbody>
</table>
HV HSIM_HV Model to Hardware Results

Excellent agreement between measured results and HiSIM_HV SPICE model.

Model features include:

- Surface potential iterative calculation used for an accurate description of drift region
- Self-heating included
- Simulation speed and accuracy is improved compared BSIM (SPICE) + subcircuit.
Layout for 50V ESD Protection

4kV ESD Cell

2kV ESD Cell
More than Moore

Moore’s Law & More

Traditional ORTC Models

Scaling (More Moore)
[Geometrical & Equivalent scaling]

Baseline CMOS: CPU, Memory, Logic

Beyond CMOS

Interacting with people and environment
Non-digital content System-in-package (SIP)

Combining SoC and SIP: Higher Value Systems

Functional Diversification (More than Moore)

Analog/RF
HV Power
Passives
Sensors
Actuators
Biochips

International Technology Roadmap of Semiconductors, ITRS 2009

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3D IC Integration

3D IC integration ... stacking of semiconductor wafers or chips using TSVs to provide electrical contact between stacked layers

TSV ... Through Silicon Via electrical contact extending through silicon

WLP ... Wafer Level Package IC packaging prior to wafer dicing

Form Factor reduction
Performance improvements
  Reduced R, C
  Reduced power consumption
  Increased speed
  Reduced signal losses (noise)

(Source: Yole Developpement, austriamicrosystems)
Ten emerging technologies to watch in 2010

9. Through silicon via

The depth of the interconnect stack on top of the leading-edge silicon surface is deep and carries a risk in minimum geometries. We have speculated that this could result in a splitting of fan-out fabrication into surface and bulk integration followed by higher-stage connection, possibly in different wafer fabs.

The desire for marketing as well as technical reasons, to mount multiple dies in single packages is also driving a need for more sophisticated interconnect and the arrival of the through-silicon via passing completely through a silicon wafer or die to clearly important in enabling 3-D packages.

In May 2009 Austria Microsystems started producing TSV parts on a foundry basis, targeting customers with 3D integration of CMOS ICs and sensor components. Expect more of the same in 2010.

10. Various battery technologies

We have become used to M楹er’s law and the steady miniaturization of microelectronics. It is easy to become frustrated with a technology that does not deliver the exponential decrease in voltage. But batteries are technology to continue.

More than Silicon: 3D-IC integration using Through Silicon Vias
3D technology concept

Top wafer processed up to last metal layer (chip1)

Bottom wafer including bond oxide (chip2)
3D technology concept

- Top wafer thinned to 250µm
- Low temperature molecular wafer bonding
- Edge removal of top wafer
Final Bonded wafer stack
3D technology concept

TSV and RDL Formation

Bumped wafer

Bump on pads - standard bump technology
3D stacking by means of TSV, BRDL and µbumps 1/3

sensor chips with µbumps

Control and read out circuit with TSV and BRDL
3D stacking by means of TSV, BRDL and μbumps 2/3

sensor chips

control and read out circuit with TSV and BRDL
3D stacking by means of TSV, BRDL and μbumps 3/3

sensor chips

control and read out circuit

printed circuit board
3D special integration tools

DRIE (STS PEGASUS)

Automated Wafer Bonder (EVG GEMINI®)

Scanning Acoustic Microscope (SONIX)

Resist Coating (EVG®150 NanoSpray)
TCAD environment set up
Key TSV reliability considerations

Defect-related (extrinsic) problems

- Defect screening
- Defect reduction

Intrinsic reliability

- Material set & construction
- Layer cracking/delamination
  e.g. TSV passivation integrity
new developments: gas sensors using 3D integration

- Temperature Sensor
- Gas transducer
- microheater
- Sensor Contacts

- CMOS wafer
- sensor wafer
- wafer bonding
- TSV processing
- top metal + TSV contacting
- TSV filling
- Handling wafer removal

Process flow for standard 3D TSV integration
3D Integrated Photodiode Array

Detection and processing of visible light intensity in CT-Scanners

- PCB
- 64 pixel Photodiode
- CMOS chip (64 channel Analog-Digital Converter)
- Transmitted x-rays from patient
- Scintillator
- Green photons
- TSV
- NMOS PMOS
Summary and Conclusions

- austriamicrosystems offers a rich portfolio of technologies tailored to high performance analog applications.

- The high voltage technologies on the 350nm and 180nm node are ideally suited for SoC applications.

- The new 3D IC integration platform(s) provide completely new ways of sensor and multiple chip solutions.

- We offer a long experience of High-Voltage CMOS/high performance analog process development and design to our customers.
Some famous last words....

Do you have it in smaller size?
Acknowledgements:

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