Bio-inspired Vision

and what electronics and computers can learn from nature

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Inspired by Biology?

- Biology: **Highly efficient** machines that greatly **outperform** any man-made technology …
- Even **small/simple animals** like the bee displays flight motor skills and cognitive behaviors, **out of reach for any artificial sensor/processor/actuator system**.
  - body weight of < 1 gram
  - brain weighing few micrograms
  - dissipating power of ~ 10µW
- Nature achieves **efficient and reliable** computation based on **fuzzy input** data in an **uncontrolled** environment
  - ➢ How is nature doing this?
  - ➢ Can we **learn** from nature?

Brain vs. Computer

Biological **brains** and digital **computers** are both complex **information processing systems**. But here the similarities end

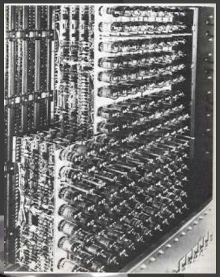
Brains:	Computers:
▪ imprecise ▪ error-prone ▪ slow ▪ flexible ▪ concurrent ▪ adaptive - tolerant of component failure ▪ autonomous learning	▪ precise ▪ deterministic ▪ fast ▪ inflexible ▪ serial ▪ susceptive to single-point failure ▪ program code

- Can understanding of brain function point the way to more **efficient, fault-tolerant** computation?
- Why is it important?

Energy Efficiency

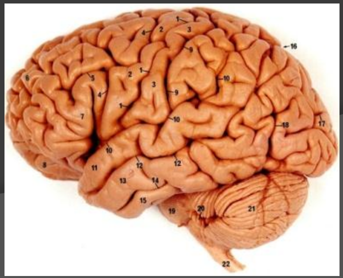
Progress of electronic information processing over past 60 years:

- dramatic improvements:
- from 5 Joules / instruction (vacuum tube computer, 1940s)
- to 0.0000000001 Joules / instruction (ARM968)
- 50,000,000,000 times better
- Raw performance increase about 1 million



Energy efficiency

- Chip: 10^{-11} J/operation
- Computer system level: 10^{-9} J/operation
- Brain: 10^{-15}J/operation
- Brain is 1 million times more energy efficient!!!



S. Furber, "The Dennis Gabor Lecture 2010: Building Brains" (2010)
C. Mead, "Neuromorphic Electronic Systems" (1990)

Where is the Energy?

1 Million

- Cost of elementary operation – turning on transistor or activating a synapse – is about the same. (10^{-15}J)
- Lose a factor 100 because:
  - capacitance of gate is a small fraction of capacitance of the node
  - spend most energy charging up wires
- Use many transistors to do one operation (typically switch 10000).
  - information encoding: “0”, “1”
  - elementary logic operations (AND, OR, NOT)

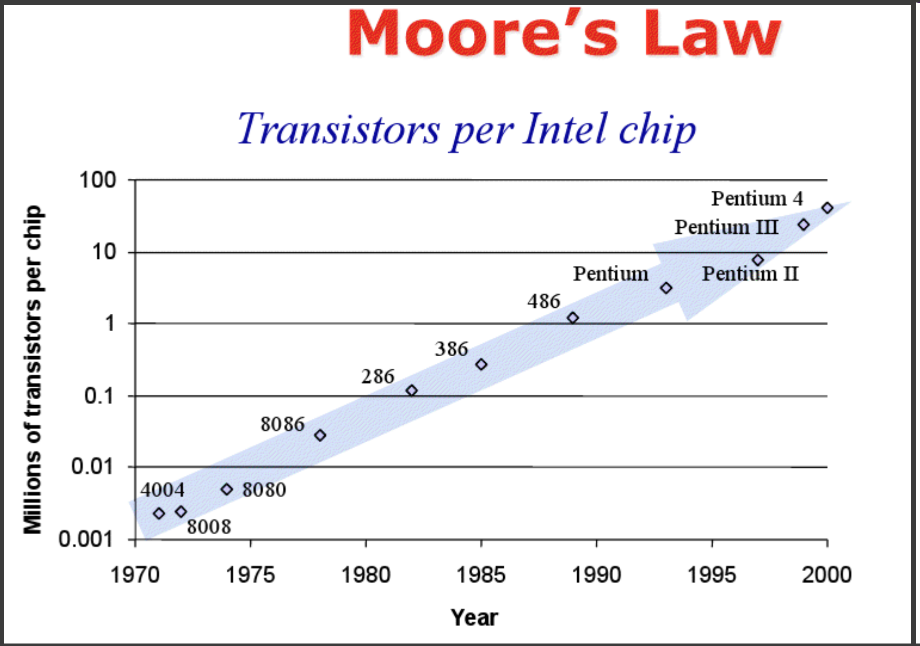
C. Mead: “We pay a *factor 10000* in energy for taking out the beautiful physics from the transistor, mash it up into “0”and “1” and then painfully building it back up with gates and operations to reinvent [e.g.] the multiplication …”

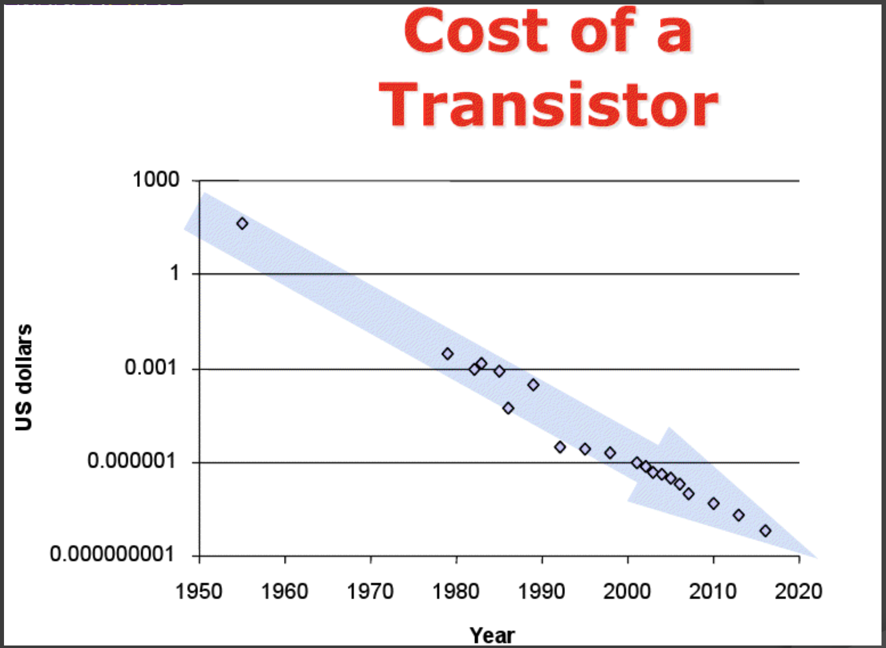
C. Mead, “Neuromorphic Electronic Systems” Proc. IEEE, (1990)

Can we get away with this?

so far we can … but for how much longer?

Credit: S. Furber, Manchester Univ.





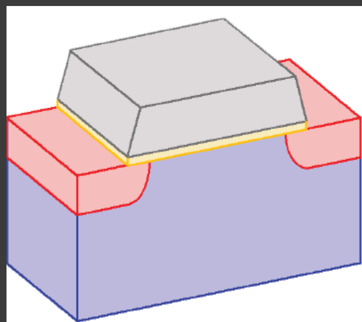
- From observation to planning tool
- Industry invests to make it happen

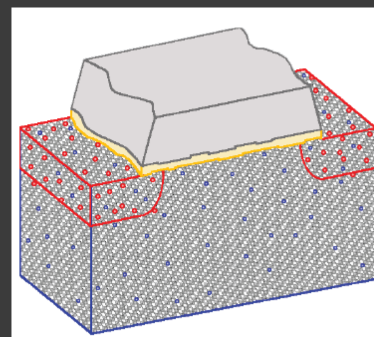
- smaller, cheaper, faster, more energy efficient

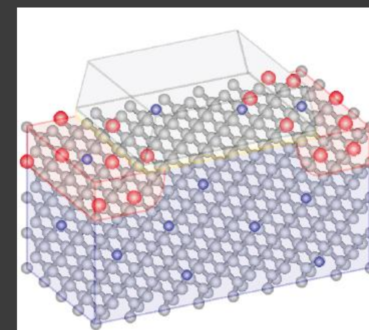
… things in silicon VLSI are getting tough …

Limitations I: Devices

5 Si-atoms / nanometer



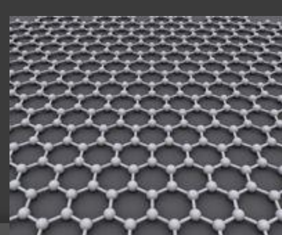


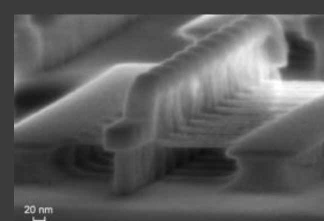


Credit: S. Furber, Manchester Univ.

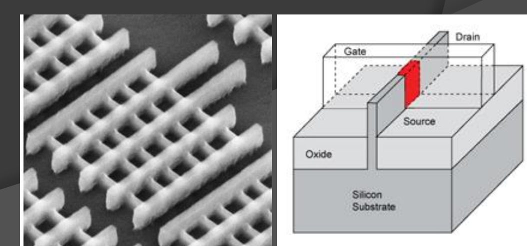
- Control of electron cloud depends critically on statistics of the components: fewer components → less robust statistics
- Transistors **less predictable, less reliable**

- Graphene transistors?
- Nano wires?
- Fin-FETS?
- Molecular transistors?





Nano-wire: IBM



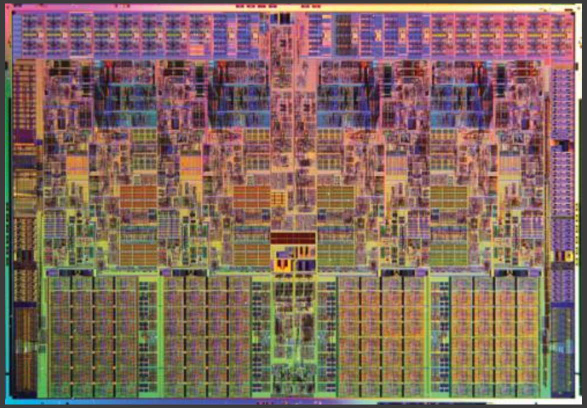
Intel Fin-FET “3D“ Transistor, May 2011

Wu, et al.“High-frequency, scaled graphene transistors on diamond-like carbon”, Nature 472,74–78, April 2011

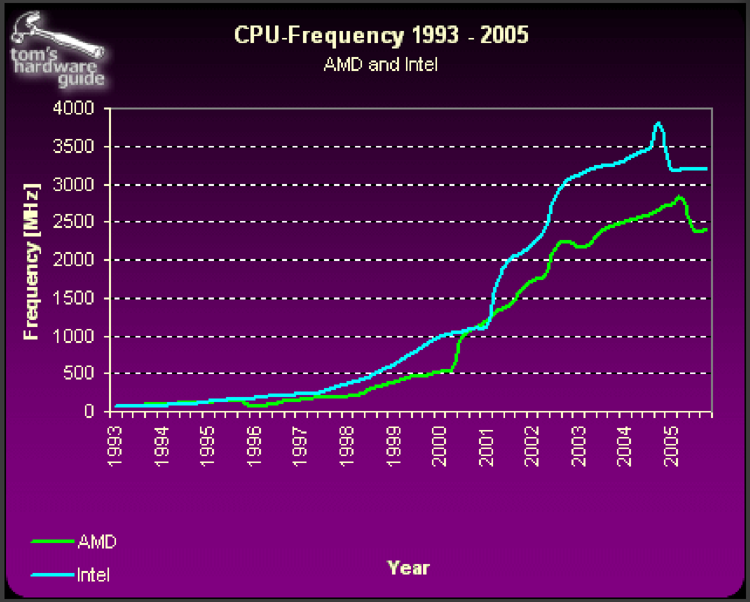
Limitations II: Computing Architecture

Clock race: Single processors running faster and faster …

- no more!!



Intel i7 quad-core (2008)

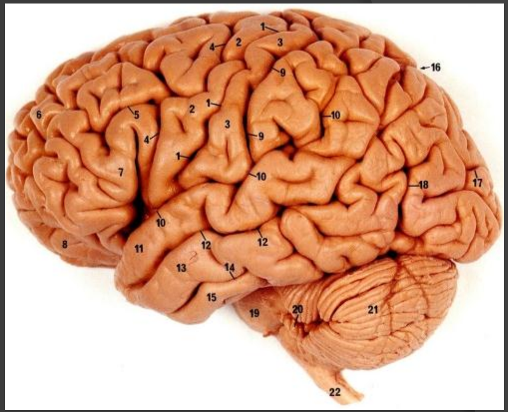


tomshardware.com

- Going parallel!
- + probably need to:
  - ➢ avoid synchronicity
  - ➢ abandon determinism

Computing Power: Human Brain vs. Computer

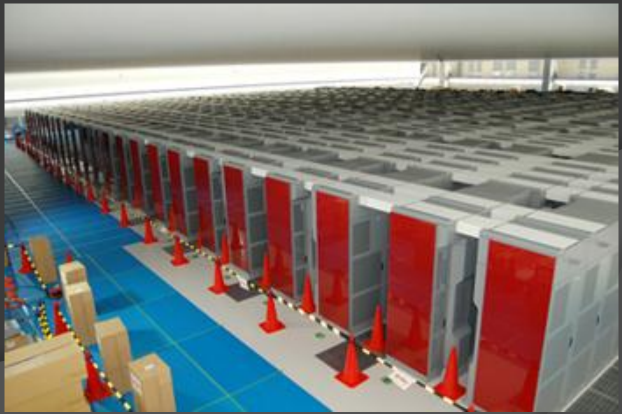
- Massive parallelism (10^{11} neurons)
- Massive connectivity (10^{15} synapses)
- Low-speed components (~1 – 100 Hz)
- >10^{16} complex operations / second (10 Petaflops!!!)
- 10-15 watts!!!
- 1.5 kg



Ellis et al. "human cross-sectional anatomy" 1991, Ed. Butterworth

„K computer“ (RIKEN, Japan)

8.162 petaflops
9.89 MW



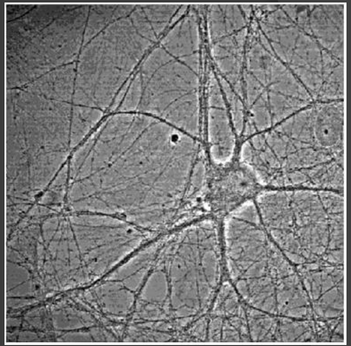
http://www.nsc.riken.jp

Biological Computational Primitive – Neuron

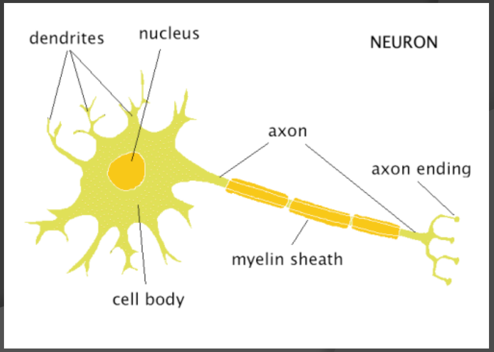
- Neurons are similar across wide range of biological brains,
- Like logic gates that are "universal" in a sense that any digital circuit can be built using the same basic gates.

Both are multiple-input single-output devices, but:

Neurons:	**Logic Gates:**
▪ fan-out: 1000-10000 ▪ dynamic, several time constants ▪ output is time-series of "spikes" ▪ fires at 10s to 100s Hz ▪ information is encoded in timing of spikes	▪ fan-out: 2-4 ▪ static internal process ▪ output is well-defined stable function of inputs ▪ defined by boolean logic



Rat hippocampal neuron
Lisa Pickard, 1999

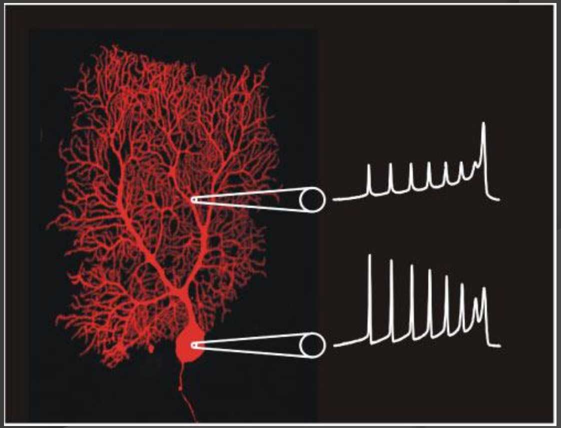


http://webspace.ship.edu/cgboer/theneuron.html

Communication and Processing

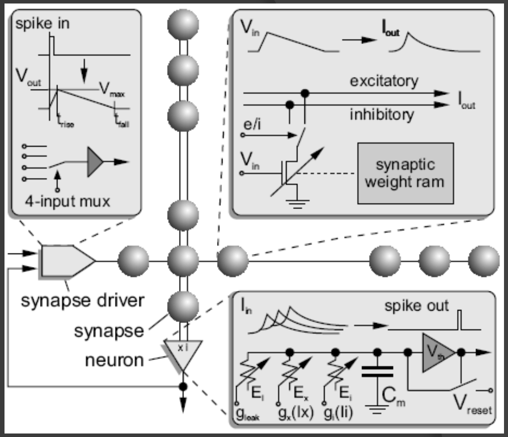
- Neurons talk to each other via of **dendrites** and **axons**
- Transmitting electrical impulses - **’spikes’** - from one neuron to another
- Most of the processing happens in the junctions between neurons – the **synapses**
- **Storage** (synapse stores state) and **processing** (evaluating incoming signal, previous state and connection strength) happen at the ***same time*** and in the ***same place***.
- This **locality** is one key to energy efficiency

Credit: Graham Johnson Medical Media



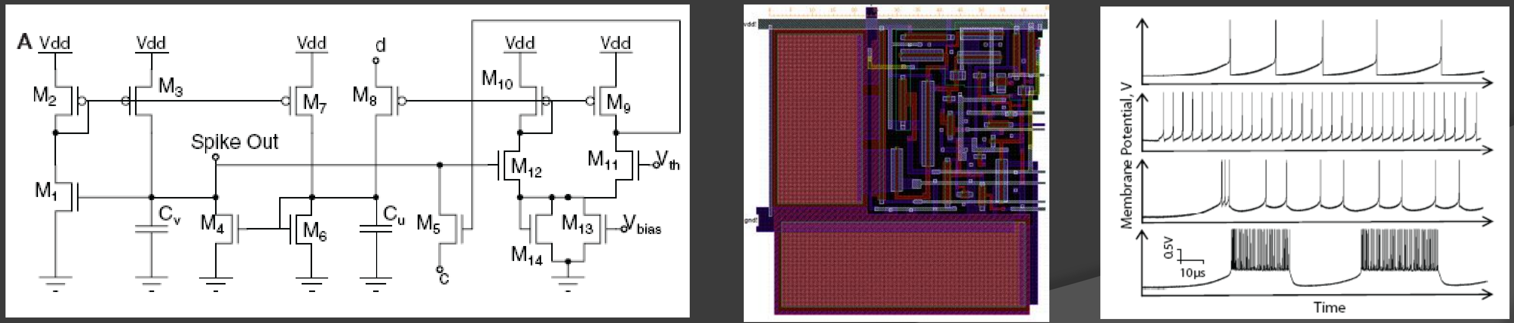
B. Mckay, University of Calgary

„Neuromorphic“ Engineering



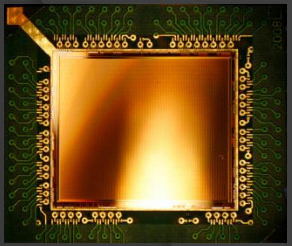
Schemmel et al., “Implementing Synaptic Plasticity in a VLSI Spiking Neural Network Model”

- C. Mead (CalTech, 1980`s – 90`s): “Neuromorphic Electronic Systems”, Proc. IEEE
- Silicon VLSI technology can be used to **build circuits** that mimic **neural functions**
- Silicon primitive: **transistor** – much physics **similar** to **neurons**
- Building blocks: **neurons, axons, ganglions, photoreceptors**, …
- Biological **computational primitives**: logarithmic functions, excitation/inhibition, thresholding, winner-take-all selection …



Wijekoon, J., et al., “Compact silicon neuron circuit with spiking and bursting behavior”. *Neural Networks. 21, 524–534.*

Building Brains



“Neurocore” - 65,536 neurons

- Mostly **limited-scale**: multi-neuron chips, synapse arrays, convolution chips etc.
- Initially for pure scientific purposes – now more and more for solving real-world **engineering and computing problems**
- Emerging technologies like **memristors** are investigated
- Some remarkable “big-scale” projects attempt the **scale** of a mammalian brain → final frontier: the **human brain**

“Neurogrid” – K. Boahen, Stanford: 1 million neurons with 6 billion synapses in mixed analog/digital VLSI.

“SpiNNaker” – S. Furber, Manchester Univ., (20 processors/chip each simulating ~1000 neurons, 65000 chips in 2D toroidal mesh)

“Brainscales/FACET” – K.H. Meier. Univ. Heidelberg: CMOS wafer-scale integration of analog multi-neuron chips (400 neurons/10000 synapses per chip, up to 10^8 neurons on the wafer system)

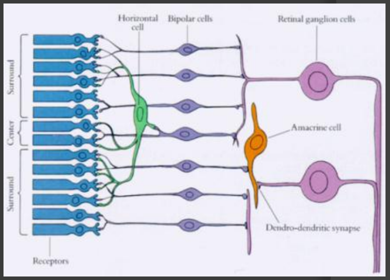
“Blue Brain” Project – Henry Markram, EPFL Lausanne → final goal: human brain running on IBM Blue Gene/L (360TFLOPS)

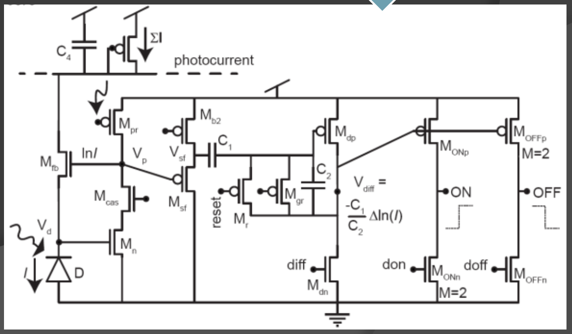
Biology-Inspired „Neuromorphic“ Vision

- Very successful branch of neuromorphic engineering: sensory transduction → vision
- **“Silicon Retina”** (Mahowald, Mead; 1989)
- Neuromorphic vision sensors sense and process visual information in a **pixel-level, event-based, frameless** manner
- Vision **processing** is practically **simultaneous** to vision **sensing**
- Only **meaningful information** is sensed, communicated, and processed

Biological Paradigm

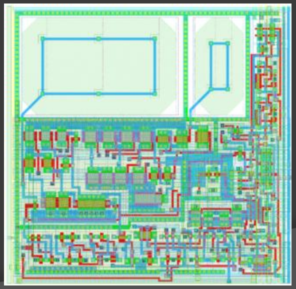
Functional Model



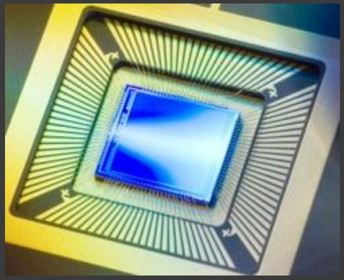


Electrical Model

VLSI Design



Neuromorphic Vision Sensor



Fukushima / NHK Research Lab 1970 Electronic Retina

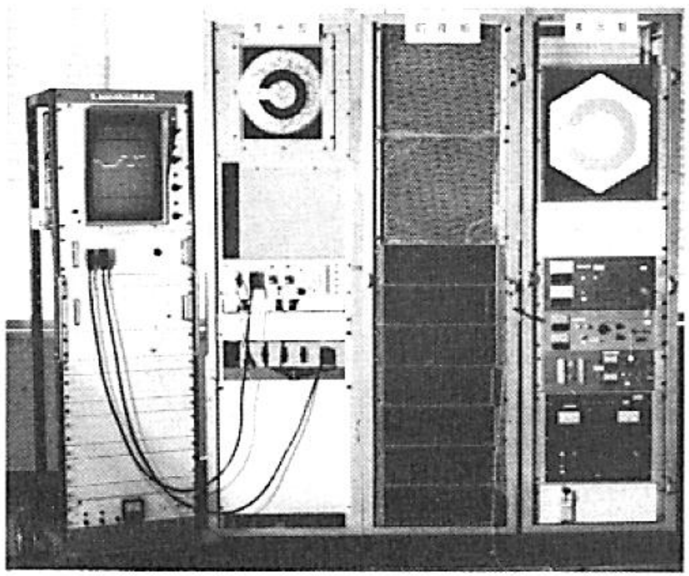
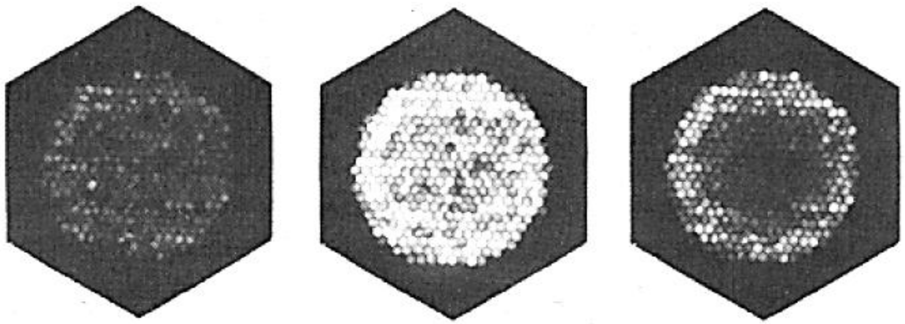


Fig. 4. Exterior view of the electronic model of the retina.



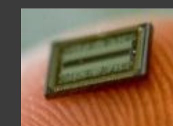
http://www4.ocn.ne.jp/~fuku_k/files/paper-e.html

K. Fukushima, et al.: "An electronic model of the retina“, *Proceedings of the IEEE*, 1970

History of integrated silicon retina vision sensors

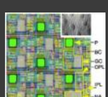
1990 — 1995 — 2000 — 2005 — 2010

Mahowald/Mead: Silicon Retina (SciAm 91)



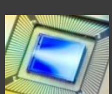
JHU/UPenn: “Octopus” imager (ISSSC 01)

CSEM: VISe contrast vision sensor (JSSC 03)

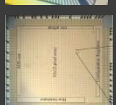


Stanford/UPenn: 5-Layer silicon retina (SciAm 05)

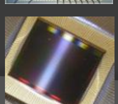
JHU: Temporal Change Detection Imager (JSSC 07)



ETH/AIT: DVS – Dynamic Vision Sensor (JSSC 08)



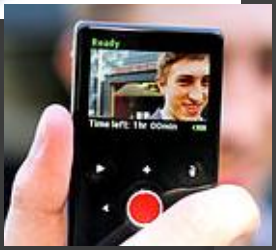
IMSE: Spatial Contrast Silicon Retina (TCAS 08)



ATIS – Asynchronous Time-based Image Sensor (JSSC 2011)

Limitations of Conventional Image Sensing

Conventional image sensors acquire the visual information as “snapshots” **time-quantized @ frame rate**

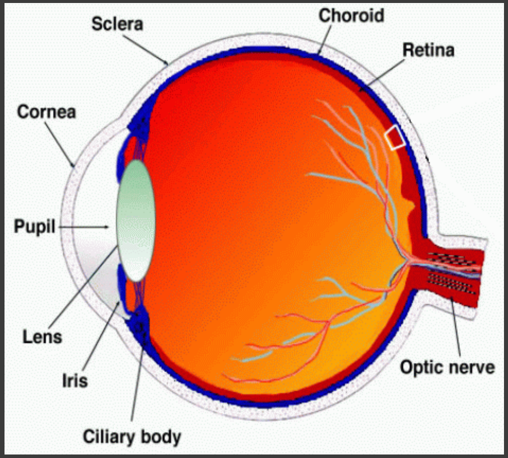


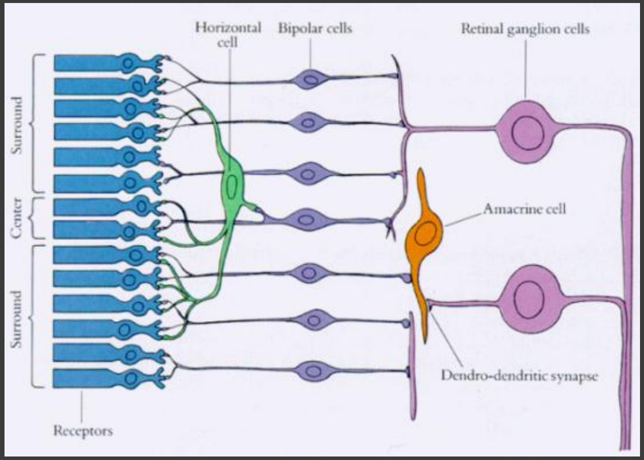
- World works in **continuous time**: things happen **between** frames
- **Each frame** carries the information from **all pixels** – whether or not this information has **changed** since the last frame

Biological approach: Not “blindly” **sense/acquire** redundant data but **respond** to visual information:

- Generate only **meaningful** data near **real-time**
- **Reduce data** rate → decrease demands on bandwidth / memory / computing power for data transmission / storage / post-processing

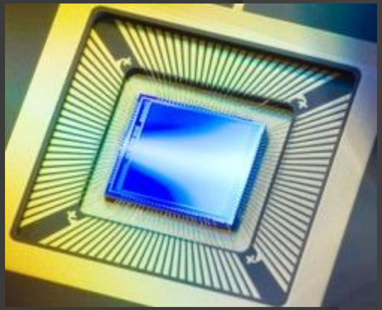
The Human Retina





- **135 million** photoreceptors – detection threshold (rod): 1 photon
- **1 million** ganglion cells in the retina **process** visual **signals** received from groups of (few to several hundred) **photoreceptors**.
- Analog **gain control**, **spatial** and **temporal filtering:** ~ 36 Gb/s HDR raw image data is compressed into ~ 20 Mb/s spiking output to the brain
- Retina encodes **useful** spatial-temporal-spectral **features** from a redundant, wide dynamic range world into a small internal signal range.
- Power consumption: ~ 3.5 mW

Biology-Inspired Dynamic Vision



Neuromorphic **Dynamic Vision Sensor (DVS)**

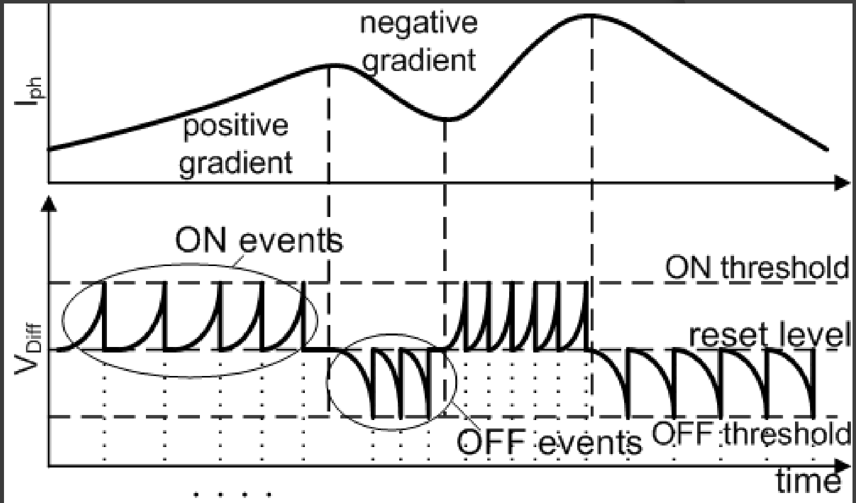
- Array of light-controlled **“integrate-and-fire” neurons** driving local **bipolar cells**
- Sensor models the Magno-cellular **transient** pathway, constitutes a simplified **three layer** model of the human retina
- **Individual pixels** respond to **relative change** (temporal contrast) by generating **asynchronous pulse events**
- **Pixels operate autonomously – no** external **timing signals** → **No frames!**
- Sensor is **event-driven** instead of **clock-driven** → responds to “natural” **events** happening in the scene
- Temporal resolution is **not quantized** to a frame-rate

Lichtsteiner, P.; Posch, C.; Delbruck, T., "A 128 × 128 120dB 30mW asynchronous vision sensor that responds to relative intensity change," **ISSCC** 2006 (**JSSC** 2008)

DVS Operation

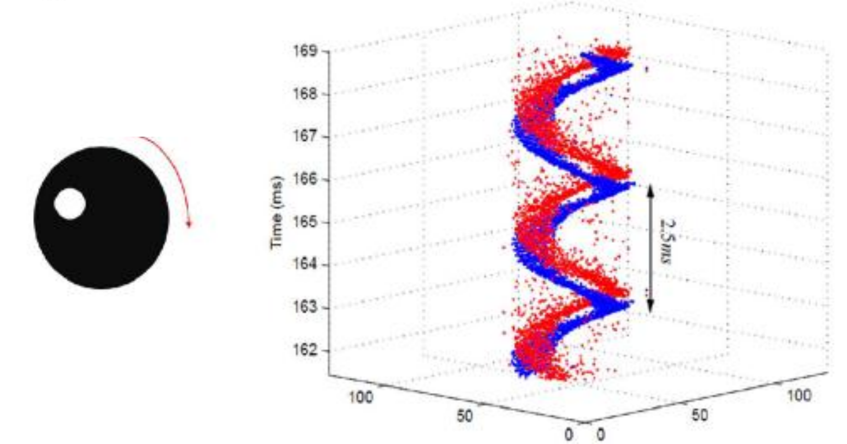
- Pixel **asynchronously** and in **continuous time** responds to **relative change** in illuminance
- Generates **‘spike’ events**
- For each spike the **x,y-address** is put on an asynchronous bus

  → **A**ddress-**E**vent-**R**epresentation



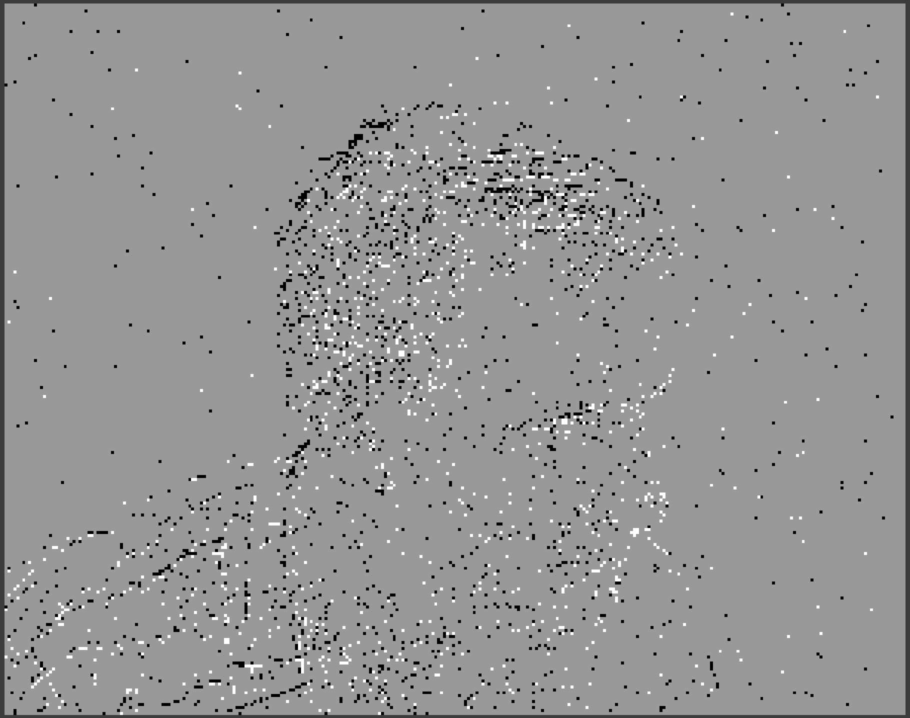
Key characteristics:

✓ Wide dynamic range (> 120dB)
✓ High temporal resolution (< 1μs)
✓ Low latency (< 10μs)
✓ High contrast sensitivity (~ 8%)



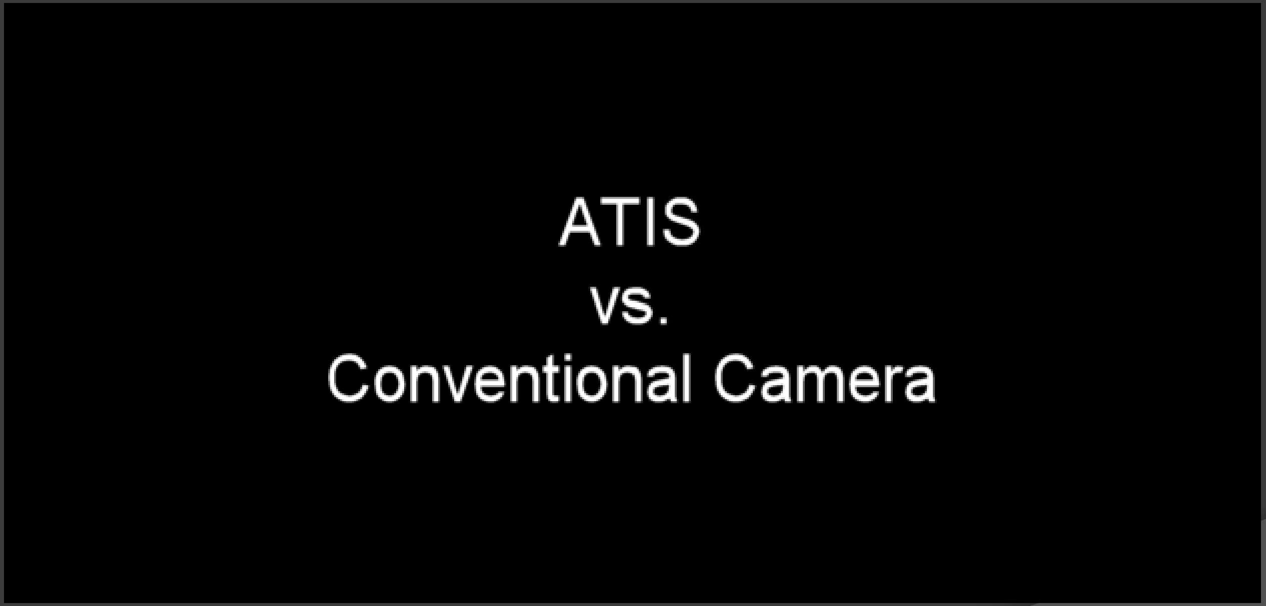
Lichtsteiner, P.; Posch, C.; Delbruck, T., "A 128 × 128 120dB 30mW asynchronous vision sensor that responds to relative intensity change," **ISSCC** 2006 (**JSSC** 2008)

Temporal Contrast Events



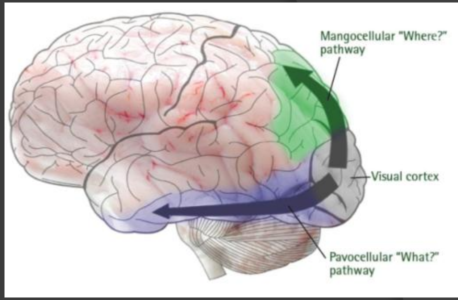
High Speed - Wide Dynamic Range

- **Temporal resolution**: µs-range (equivalent 100`000 to 1`000`000 frames/s)
- **Dynamic range** >120 dB (standard CMOS/CCD: 60 – 70dB)

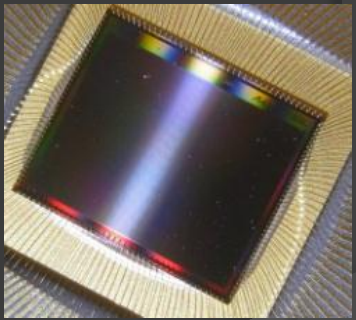


Next-generation bioinspired imaging „where“ and „what“!

Magno- and **Parvo-** ganglion cells –
have very different spatio-temporal characteristics



- **Transient** Magno-cellular pathway – alerting → **“where” system**
- **Sustained** Parvo-cellular pathway – detailed vision → **“what” system**
- Next step: Add biological **“What”** function to transient temporal contrast sensing.



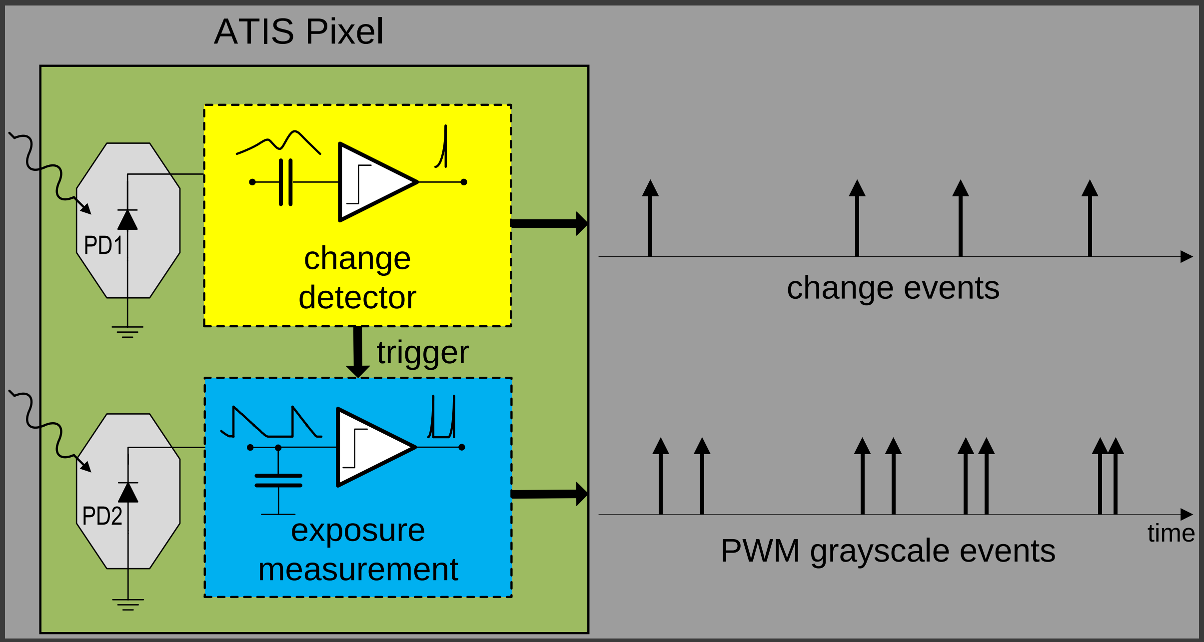
- **Sustained pathway** principle encodes **absolute** intensity (gray-levels) in asynchronous pulse events.

→ Array of **pixels** that:

- **individually** and **autonomously** react to scene changes <u>and</u>
- acquire illumination information **conditionally** and **event-driven**

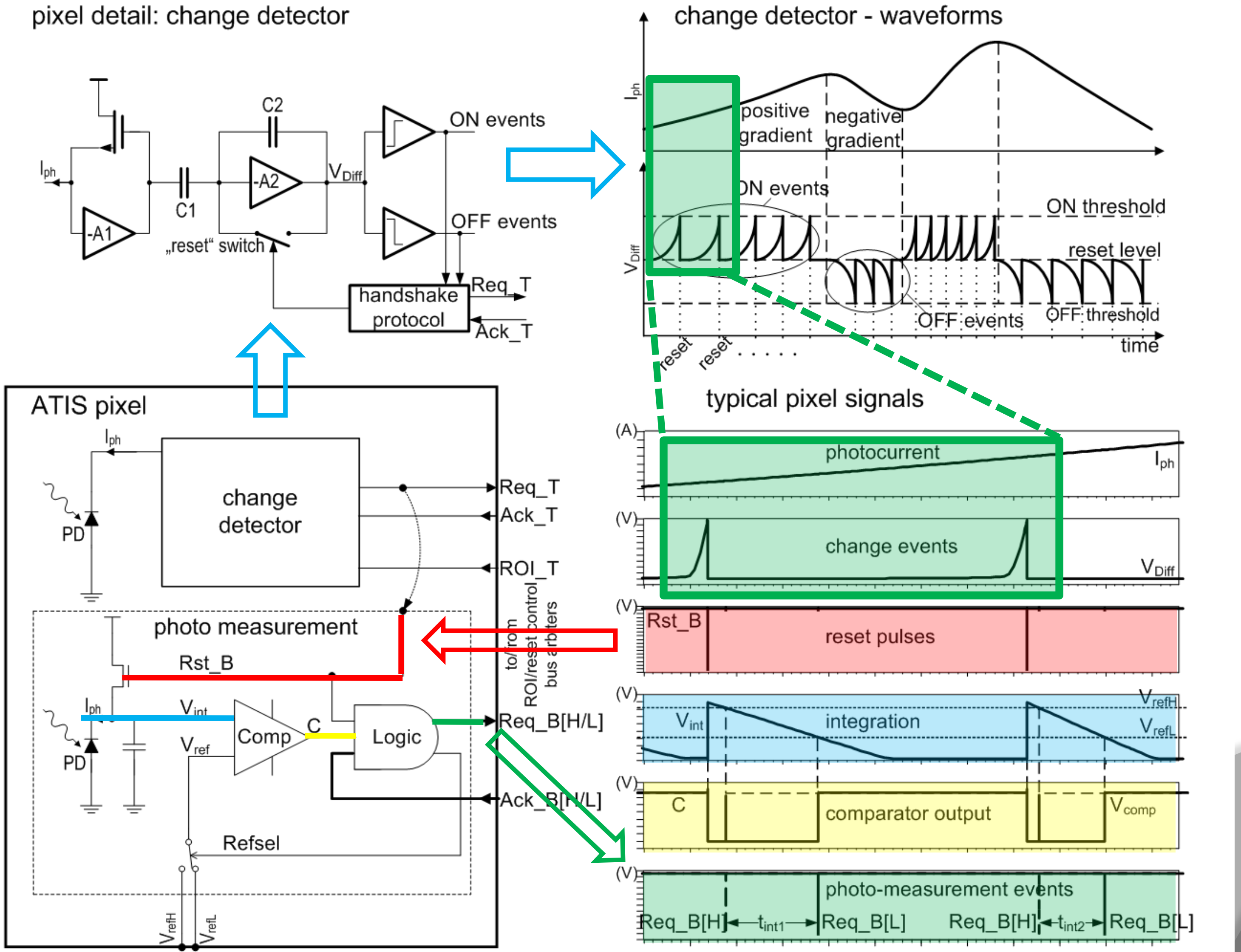
Asynchronous **T**ime-based **I**mage **S**ensor – **ATIS**

ATIS Pixel – Basics



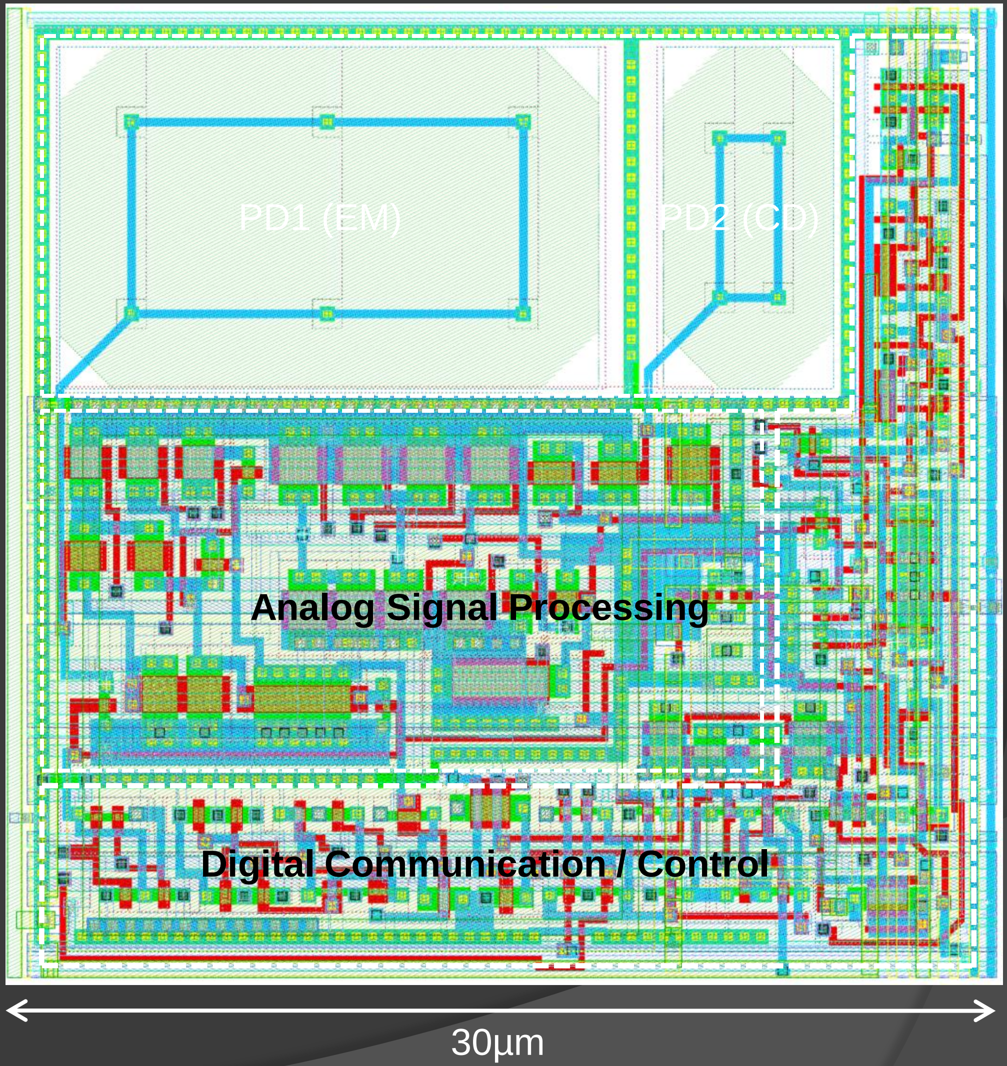
- Two blocks: **DVS change detector** and **exposure measurement**
- **Change detector triggers** exposure measurement **only after** a detected change in the pixel`s FoV
- **Continuous-time asynchronous** operation
- Communicates detected **changes** AND **new** exposure information **independently** and **asynchronously – NO FRAMES**
- Intensity-encoding is **time-based**

ATIS Pixel – The Complete Picture

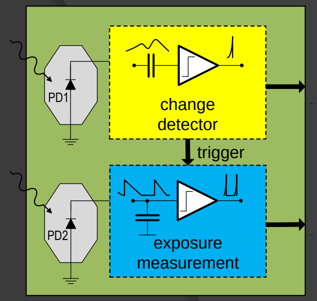


ATIS Pixel Layout – CMOS 0.18µm

- 0.18µm CMOS
- 30 × 30µm²
- 77T, 4C, 2 PDs
- Fill factor: 30%
  10% CD
  20% EM
- Analog part:
  - change detector
  - integration
  - comparator
- Digital part
  - pixel-level state logic
  - communication
  - handshaking



ATIS Concept – Implications



Pixel-autonomous change-detector controlled operation

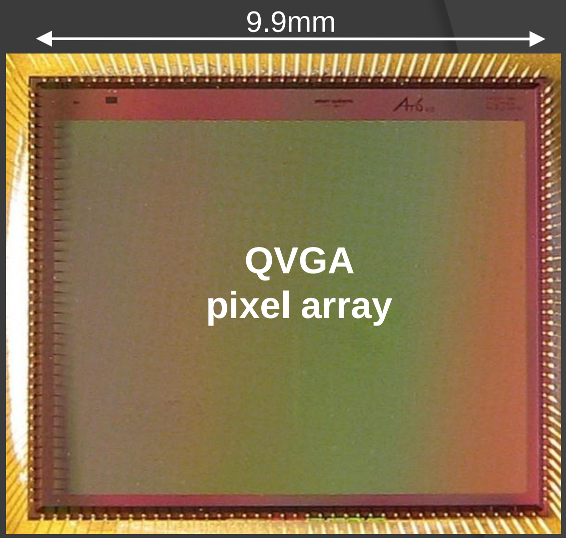
- Pixel does not rely on **any** external timing signals
- Pixel that is **not stimulated** visually does **not produce output**
- Complete **suppression** of temporal data **redundancy** = **lossless pixel-level video compression**

Asynchronous time-based encoding of exposure information

- **Avoids** the **time quantization** of frame-based acquisition and scanning readout.
- Allows **each pixel** to **choose** its own optimal **integration time** instead of imposing a fixed integration time for the entire array.
- Yields exceptionally **high dynamic range** (DR) and improved **signal-to-noise-ratio** (SNR).
- DR is **not limited** by power **supply rails**

ATIS – Specifications

Fabrication process	UMC L180 MM/RF 1P6M CMOS
Supply voltage	3.3V (analog), 1.8V (digital)
Chip size	9.9 × 8.2mm^2 (6.8 Mio. transistors)
Optical format	2/3“
Array size	QVGA (304 × 240)
Pixel size	30µm × 30µm
Pixel complexity	77T, 3C, 2PD
Fill factor	30% (20% EM, 10% CD)
Integration swing ΔV_{th}	100mV to 2.3 V (adjustable)
SNR typ.	>56dB (9.3bit) @ ΔV_{th} = 2V, >10Lx
SNR low	42.3dB (7bit) @ $\Delta V_{th\ min}$ (100mV), 10Lx
t_{int} @ $\Delta V_{th\ min}$ (100mV)	2ms @ 10Lx (500 fps equ. temp. res.)
DR (static)	143dB
DR (30fps equivalent)	125dB
PRNU / FPN	<0.25% @ 10Lx (with TCDS)
Power consumption	50mW (static), 175mW (high activity)
Readout format	Asynchronous AER, 2 × 18bit-parallel



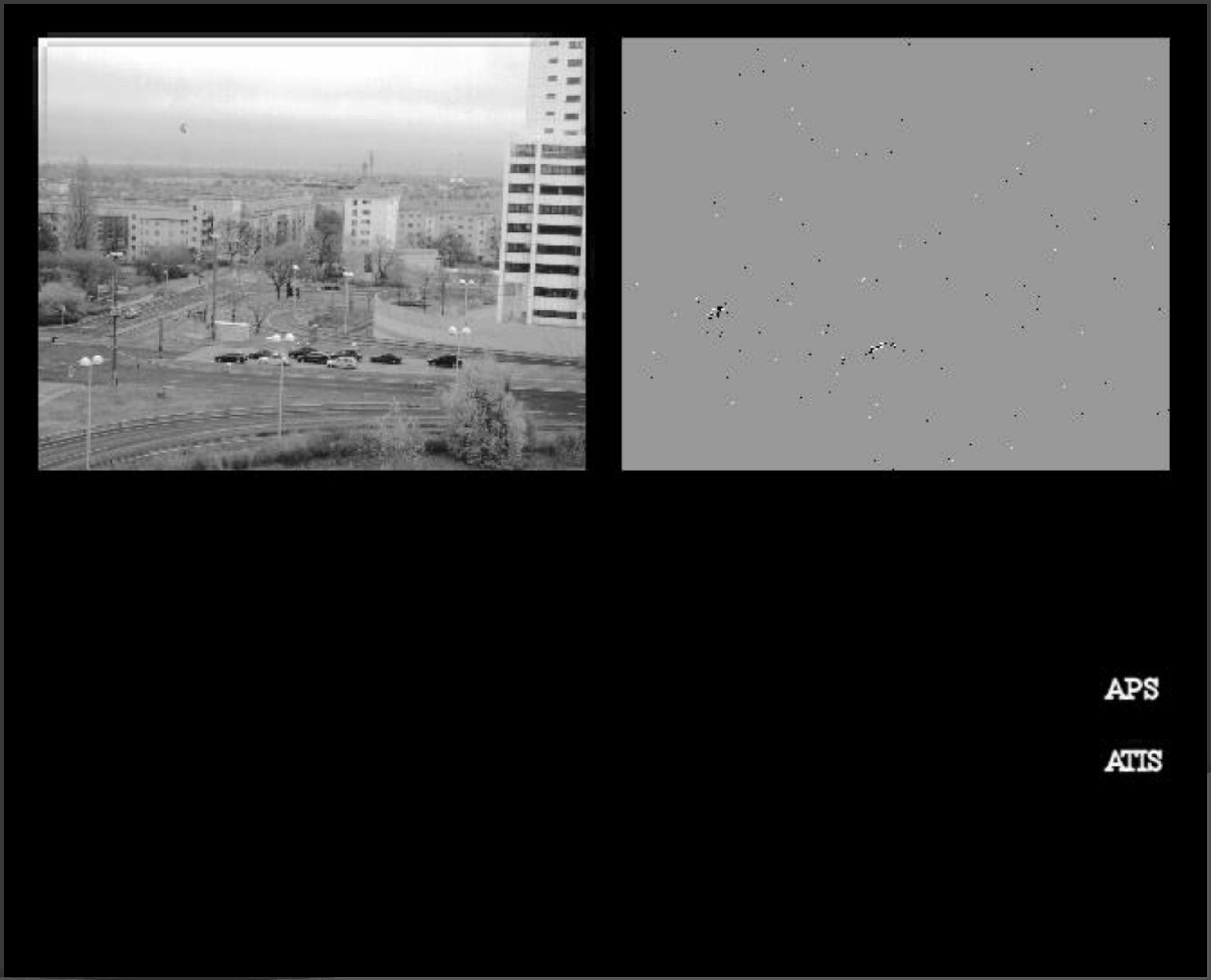
Ultrahigh Dynamic Range

- **143dB** for **static scene**
- **125dB for 30fps** (video speed) equivalent temporal resolution

Pixel-level Video Compression

- QVGA continuous-time video stream
- 2.5k – 50k events/sec
- with 18bit/event
  45k – 900k bit/sec
- 30fps × 8bit × QVGA
  = 18Mbit/sec (raw)
- Variable compression factor: **20 – 400**

Behind the Scenes



Conclusions

DVS real-time contrast data

- ✓ Wide dynamic range (> 120dB)
- ✓ High temporal resolution (< 1µs)
- ✓ Low latency (< 10µs)
- ✓ Contrast sensitivity ≥ 10%

<u>High-speed dynamic machine vision</u>

- Industrial robotics
- Micromanipulation
- Autonomous robots and AUVs
- Automotive

… where need for speed meets uncontrolled lighting conditions!

ATIS frame-free, compressed video

- ✓ Wide dynamic range (125–143 dB)
- ✓ Fast (500 fps equ.temp.res. @ 10lx)
- ✓ High image quality (56dB SNR)
- ✓ Compression up to 1000 (static)

<u>Low-data rate video</u>

- Wireless sensors
- Sensor networks
- Web video

<u>Wide DR, high-quality imaging/video</u>

- Cell monitoring
- X-ray crystallography
- Astronomy

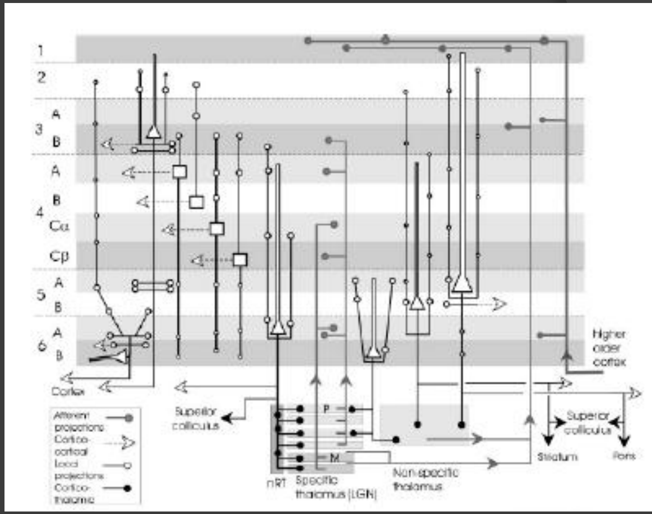
Thank you for your attention!

Outline

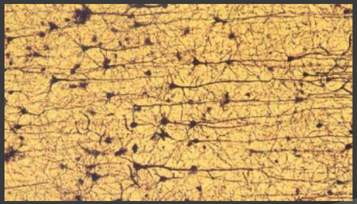
- Bio-inspired?
- Computers and brains: similarities and differences
- Limitations to digital, synchronous information processing
- Computational primitives – neurons vs. logic gates
- “Neuromorphic Engineering” – building brains
- Vision – biological / bio-inspired
- Modeling the retina – ”Silicon Retina”
- CMOS implementations of bio-inspired vision chips
- Applications
- Outlook

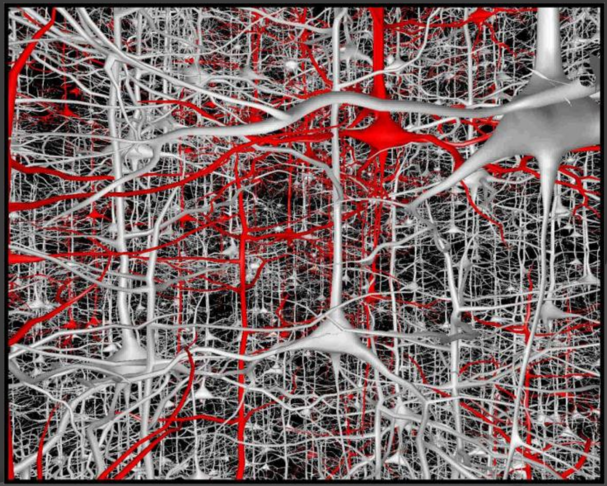
Neural Circuits – Cortical Architecture

- **Regular high-level** structure
  - e.g. 6-level cortical micro architecture
    - low-level vision
    - language, …



- **Random low-level** structure
  - adapts over time
  - synaptic connections change
  - weights change
  - → **learning!!**





Brain Mind Institute, EPFL

Brain vs. Computer - II

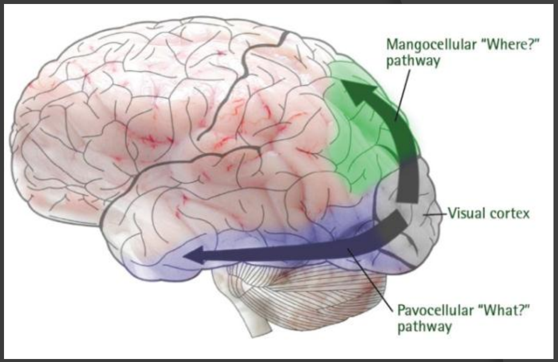
At the system level, brains are at least **1 million times more power efficient** than computers. **Why?**
Cost of elementary operation (turning on transistor or activating synapse) is **about the same**. It's not some magic about physics. (10^{-15} J)

Computer	Brain
Fast global clock	Self-timed, data driven
Bit-perfect deterministic logical state	Synapses are stochastic! Computation dances digital→analog→digital
Memory distant to computation	Synaptic memory at computation
Fast, high resolution, constant sample rate analog-to-digital converters	Low resolution adaptive data-driven quantizers (spiking neurons)

Mobility of electrons in silicon is about **10^7 times** that of ions in solution.

T. Delbruck, "Spiking silicon retina for digital vision". IEEE DLP lecture

Biological Vision – Retina Ganglion Cells



Two different types of retinal ganglion cells and corresponding retina-brain pathways:

Magno- and **Parvo-Cells** –
very different spatio-temporal characteristics

Magno-cellular pathway – **transient channel**

- receptors *evenly distributed* over retina, big (low spatial resolution)
- *short latencies*, rapidly conducting axons (high temporal resolution)
- respond to *changes*, movements, onsets, offsets (transient response)
- biological role in *alerting*, detecting dangers in our peripheral vision
- **“Where” system**

Parvo-cellular pathway – **sustained channel**

- receptors concentrated in the fovea, *small* (high spatial resolution)
- have *longer latencies* and slower conducting axons (low temporal res.)
- respond as long as *visual stimulus is present* (sustained response)
- transportation of *detailed* visual *information* (spatial details, color)
- **“What” system**

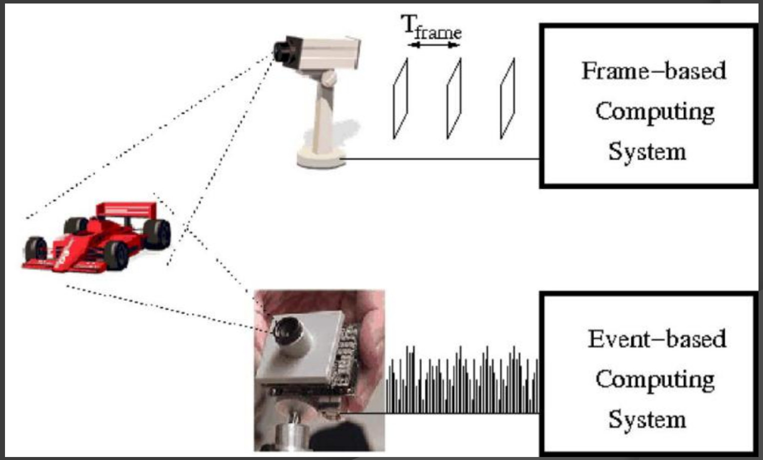
(A. v.d.Heijden, „Selective attention in vision“)

Bioinspired Vision – Events vs. Frames

- Conventional imagers:
  - **Neglect dynamic** visual information
  - Acquire **frames** at discrete points in time

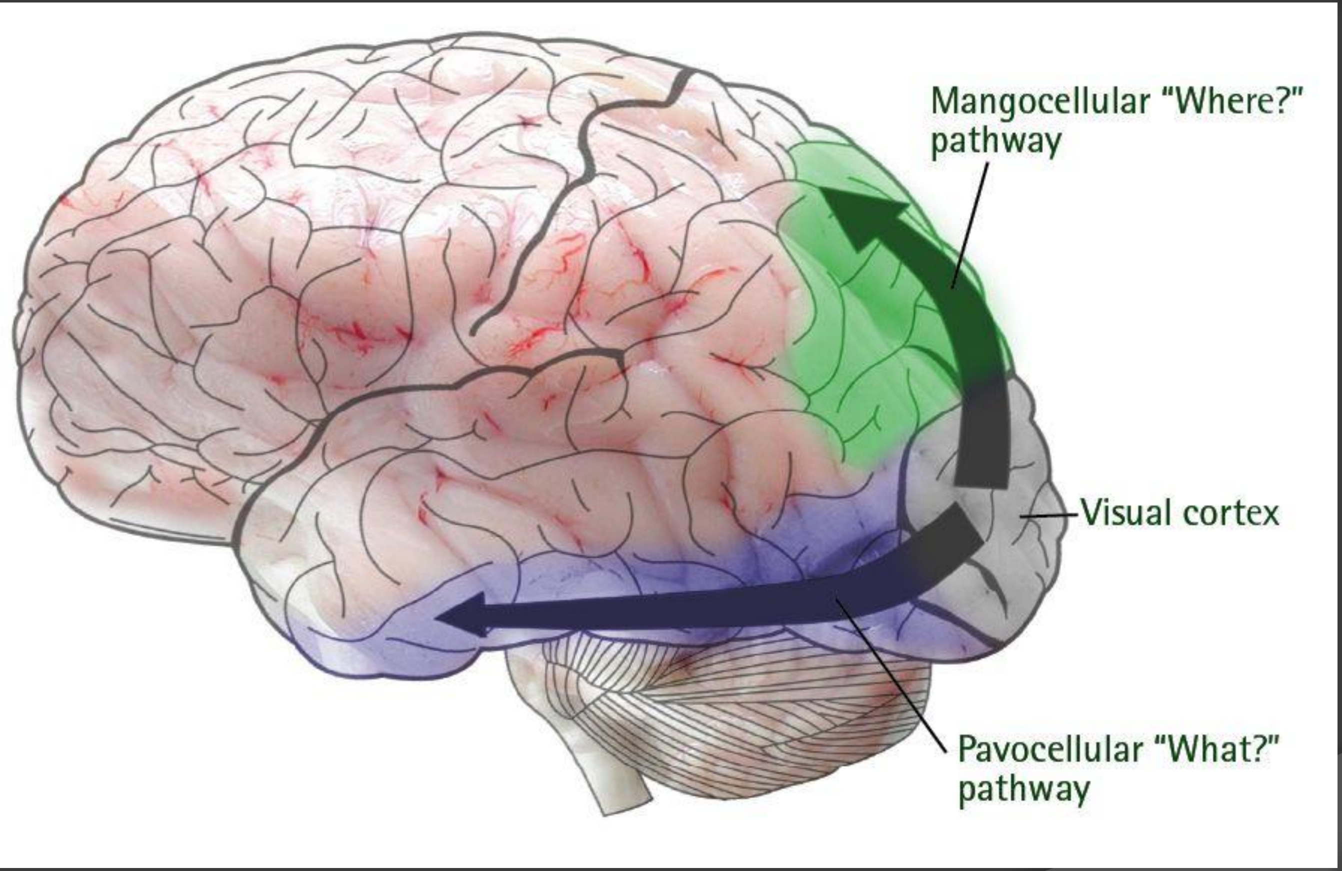
- A lot of interesting **information** in the **dynamic** contents of a **scene**
- Things happen between frames …
- New paradigm of visual sensing and processing

→ **“Event-based vision”**



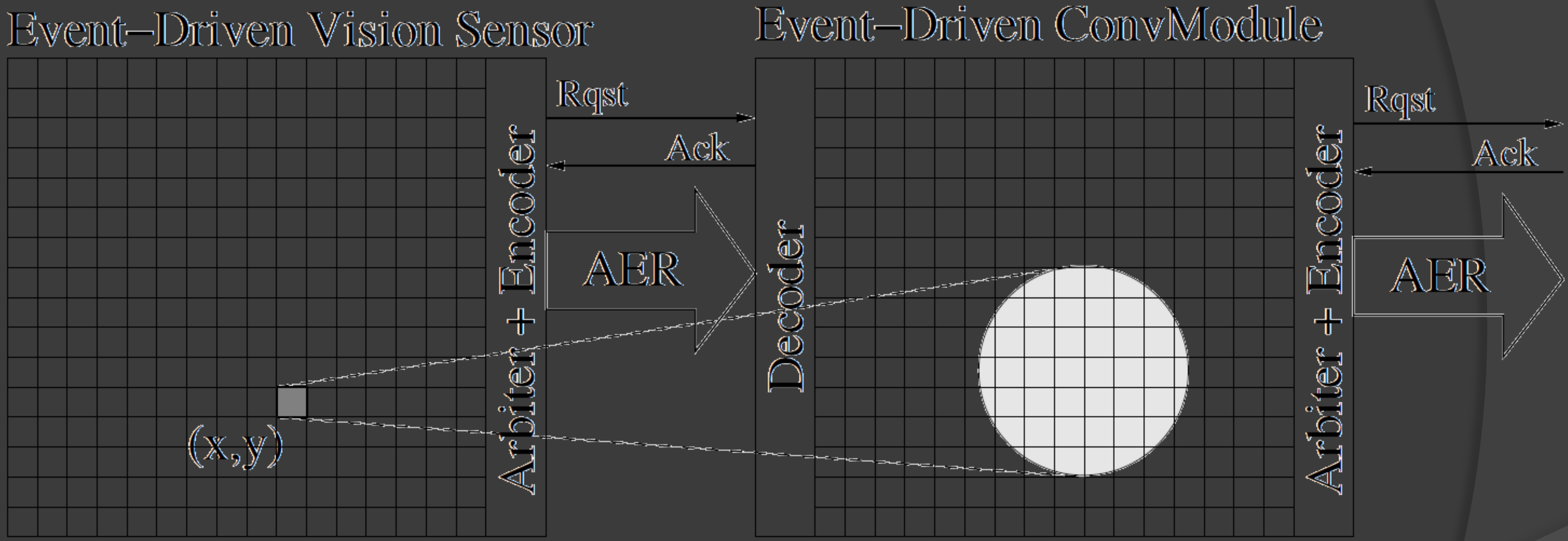
Pérez-Carrasco et al., “Fast Vision Through Frameless Event-Based Sensing and Convolutional Processing”, TNN 2010

Going past the retina and simple vision



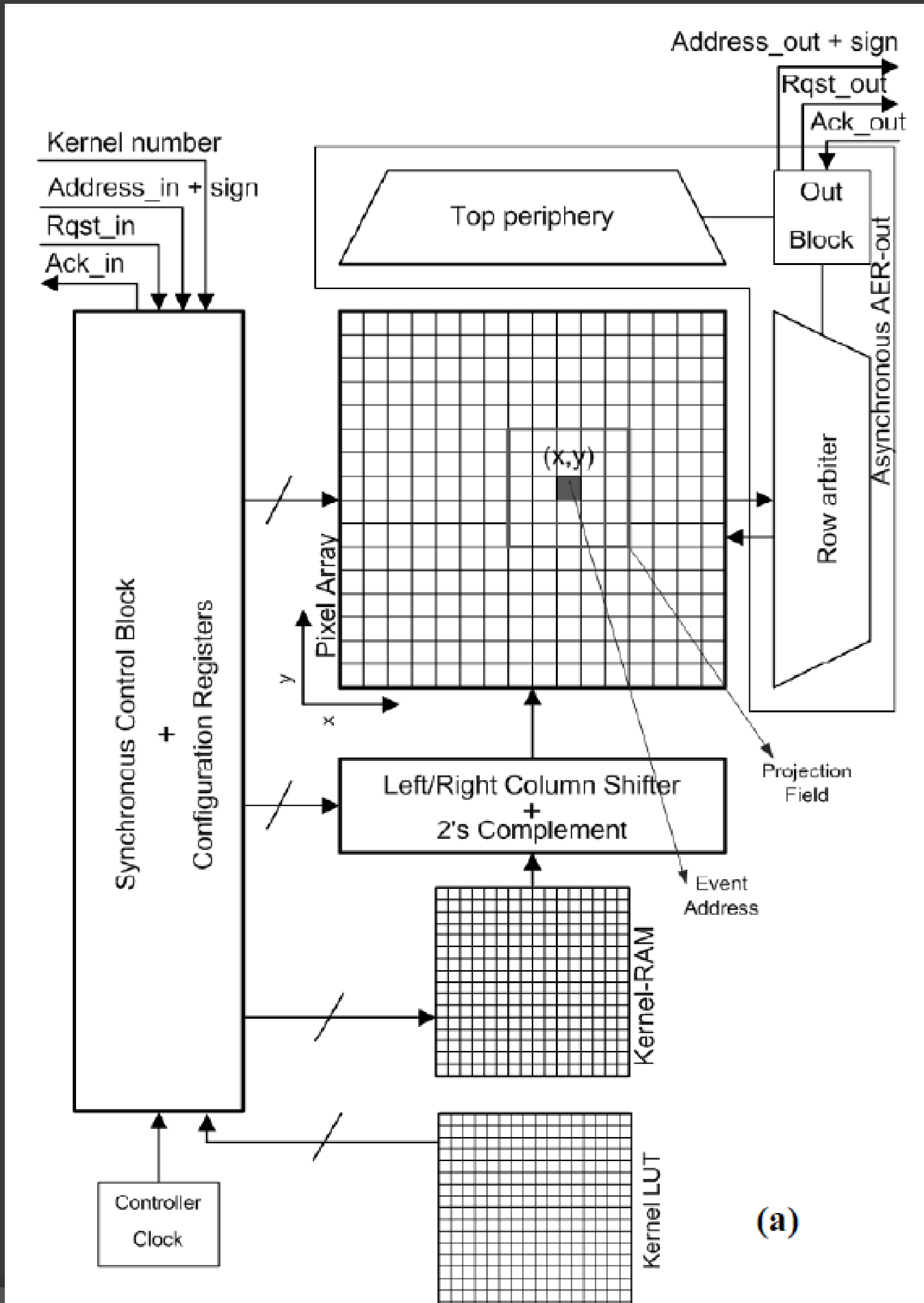
Event-based Visual Cortex – Convolution

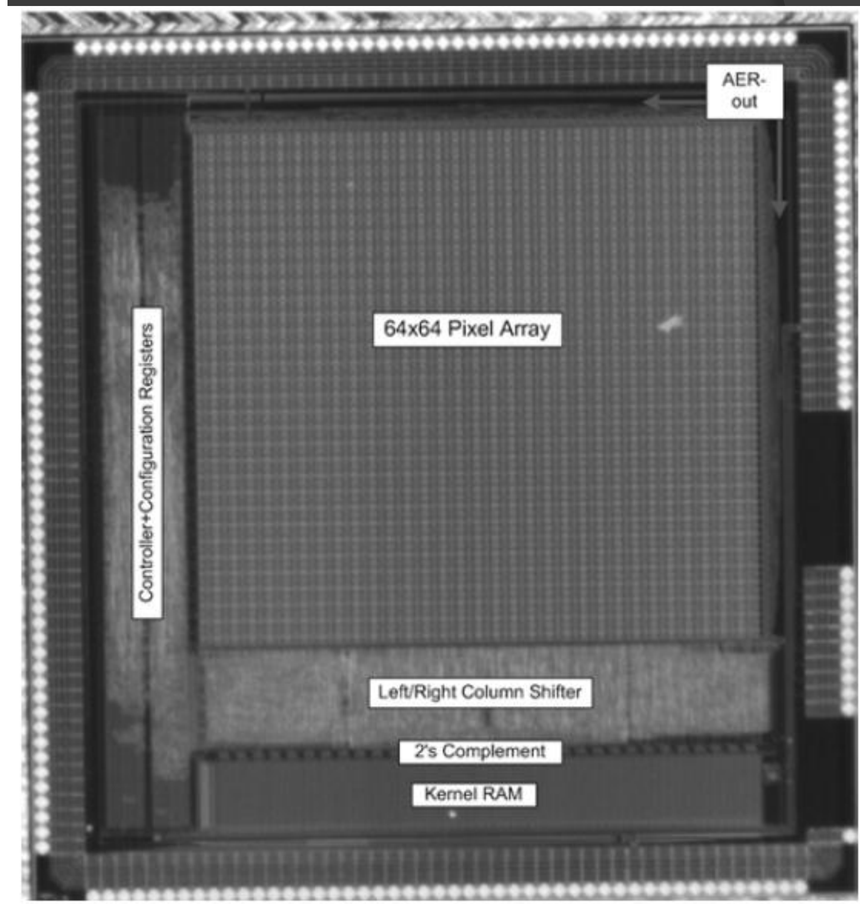
Projective AER convolution hardware module



AER=Address-Event Representation

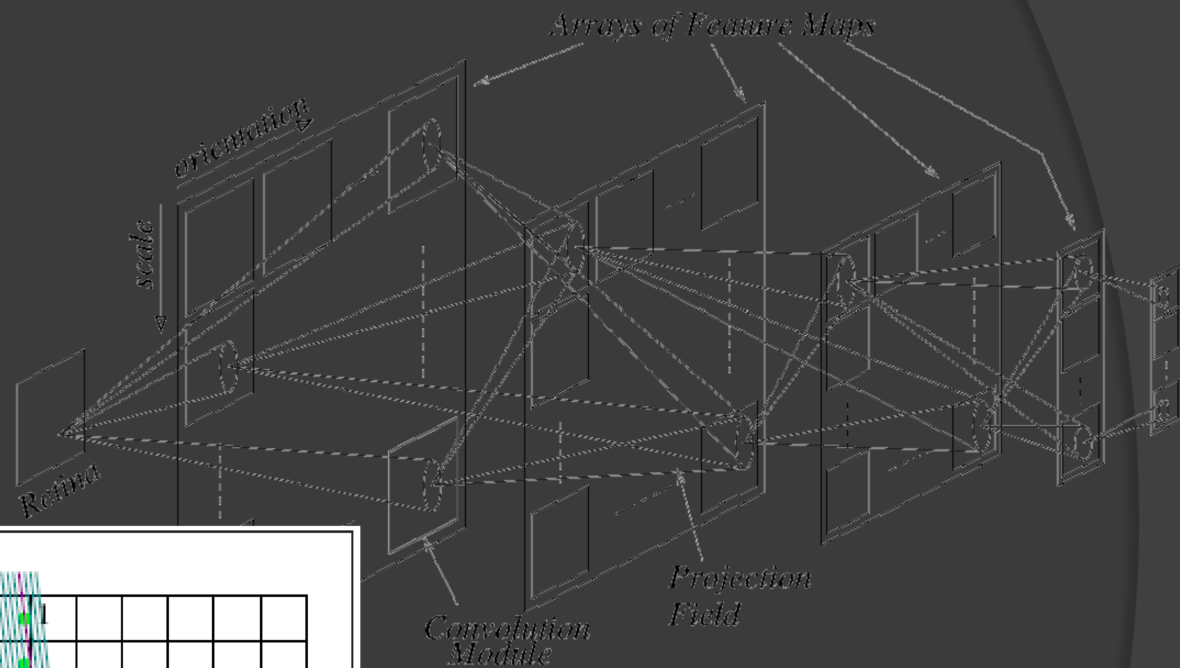
64x64 ConvModule





L. Camunas-Mesa et al., 2010

Building a Self-Learning Visual Cortex with Memristors



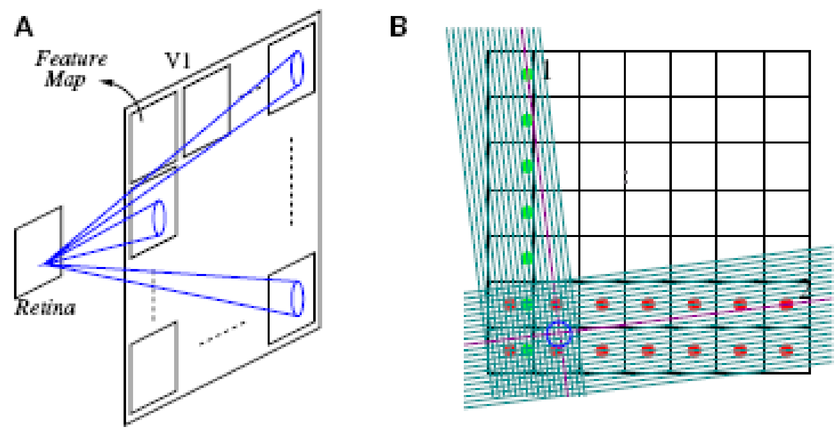


FIGURE 21 | (A) Projection Field Topology of V1 layer in Visual Cortex.
(B) Hybrid CMOS-memristor arrangement with CMOL style tilted lines.


time = 0s
time=84402s
time=168804s
time=844020s

Selected publications

- Posch, C.; Matolin, D.; Wohlgenannt, R., "A QVGA 143dB Dynamic Range Frame-free PWM Image Sensor with Lossless Pixel-level Video Compression and Time-Domain CDS", *IEEE Journal of Solid-State Circuits,* vol. 46, no. 1, pp. 259-275, Jan 2011. **(invited)**
- Posch, C.; et al. "Live Demonstration: Asynchronous Time-Based Image Sensor (ATIS) Camera with Full-Custom AE Processor", *Circuits and Systems, ISCAS 2010. IEEE International Symposium on*, May 2010. "**ISCAS 2010 Best Live Demonstration Award"**
- Chen, D.; Matolin, D.; Bermak A.; and Posch, C., "Pulse Modulation Imaging - Review and Performance Analysis", *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 1, pp. 64-82, Jan 2011.
- Posch, C.; Matolin, D.; Wohlgenannt, R., "A QVGA 143dB DR Asynchronous Address-Event PWM Dynamic Image Sensor with Lossless Pixel-Level Video Compression," *Solid-State Circuits, 2010 IEEE International Conference ISSCC*, pp. 400-401, Feb. 07-11, 2010.
- D. Matolin, C. Posch, R. Wohlgenannt, "True Correlated Double Sampling and Comparator Design for Time-Based Image Sensors", *Circuits and Systems, IEEE International Symposium on, ISCAS 2009.* **"ISCAS 2009 1st Honorary Mention SSTC Best Paper Award"**
- C. Posch, D. Matolin, R. Wohlgenannt, "A Two-Stage Capacitive-Feedback Differencing Amplifier for Temporal Contrast IR Sensors", *Electronics, Circuits and Systems, 2007. IEEE International Conference on*, *ICECS 2007.* **"ICECS 2007 Best Paper Award"**
- Lichtsteiner, P.; Posch, C.; Delbruck, T., "A 128 × 128 120dB 15us Latency Asynchronous Temporal Contrast Vision Sensor", *JSSC, IEEE Journal of Solid-State Circuits*, 2008.
- Posch, C.; Hofstätter, M.; Matolin, D.; Vanstraelen, G.; Schön, P.; Donath, N.; Litzenberger, M., "A dual-line optical transient sensor with on-chip precision time-stamp generation," *Solid-State Circuits, 2007 IEEE International Conference, Digest of Technical Papers*, *ISSCC 2007.*
- Lichtsteiner, P.; Posch, C.; Delbruck, T., "A 128 × 128 120db 30mW asynchronous vision sensor that responds to relative intensity change," *Solid-State Circuits, 2007 IEEE International Conference, Dig. of Technical Papers*, *ISSCC 2006.* **"ISSCC 2006 Jan Van Vessem Award for Outstanding European Paper"**

Patents: ÖPA 504.582, ÖPA 502.032, PCT/AT2006/000203, ÖPA A1940/2006, ÖPA A1628/2007

Applications of DVS

DVS events are well suited to drive computer vision systems

- Fast visual feedback loops
- Motor control
- Industrial robotics
- Autonomous robots and AUVs
- Automotive

… where **need for speed** meets **uncontrolled lighting conditions**!

AIT AUSTRIAN INSTITUTE OF TECHNOLOGY applies DVS in

- Traffic data acquisition
- People counting, people flow monitoring
- Ambient assisted living (fall detection)
- Gesture recognition

Event-based vs. Frame-based Processing

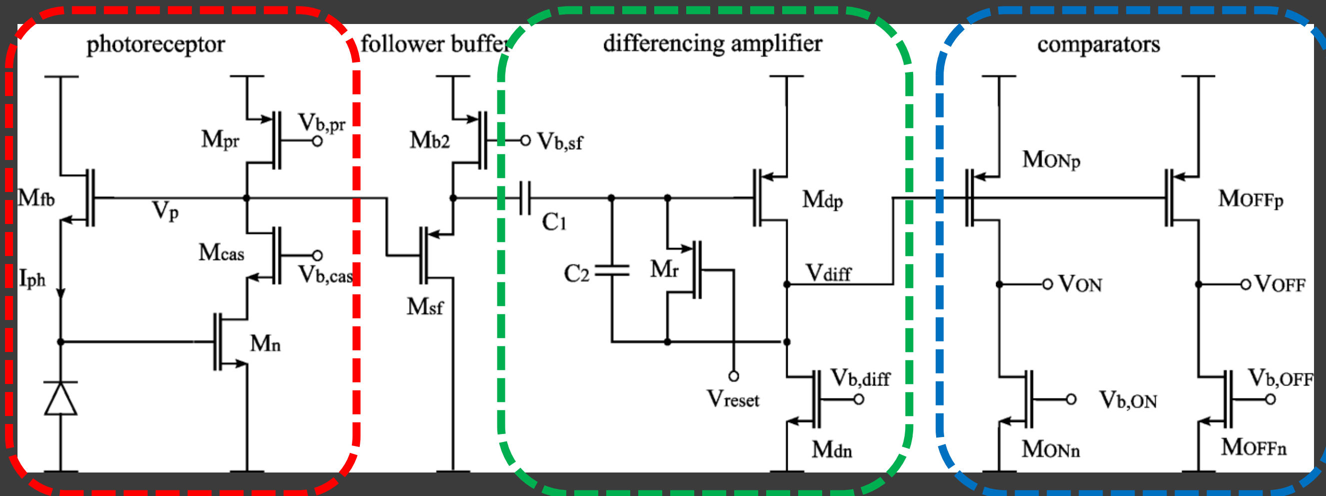
Frame-based (conventional)

- camera captures a sequence of frames
- each frame is transmitted to a computing system
- processed by sophisticated image processing algorithms for achieving some kind of recognition
- computing system needs to have all pixel values of a frame before starting any computation
- reality is binned into compartments of duration T_{frame}
- computing system has to process the full frame, handling large amounts of data

Event-based (bio-inspired)

- pixel sends an event (usually its own x,y coordinate) when it senses something – asynchronous, real-time
- events are transferred to computing system as they are produced
- computing system updates its state after each event
- events are processed as they flow – sensing and processing is done concurrently – no need to wait for frames
- For performing recognition not all events are necessary

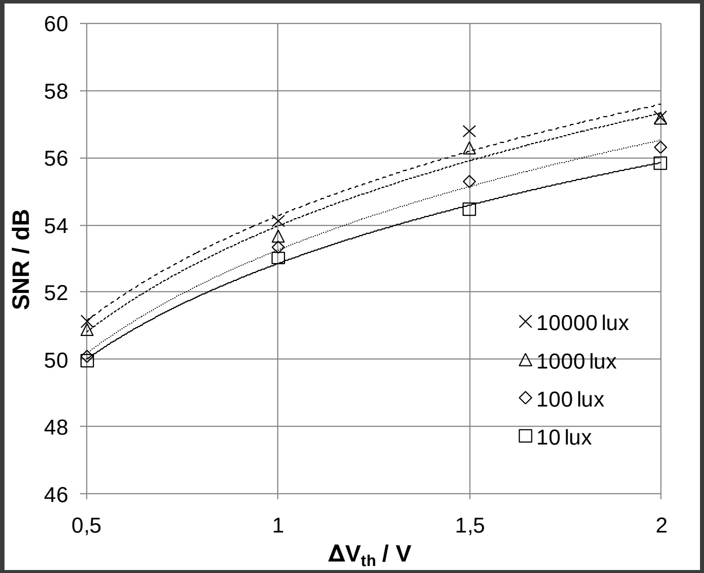
Pixel circuit – "Integrate-and-Fire" neuron

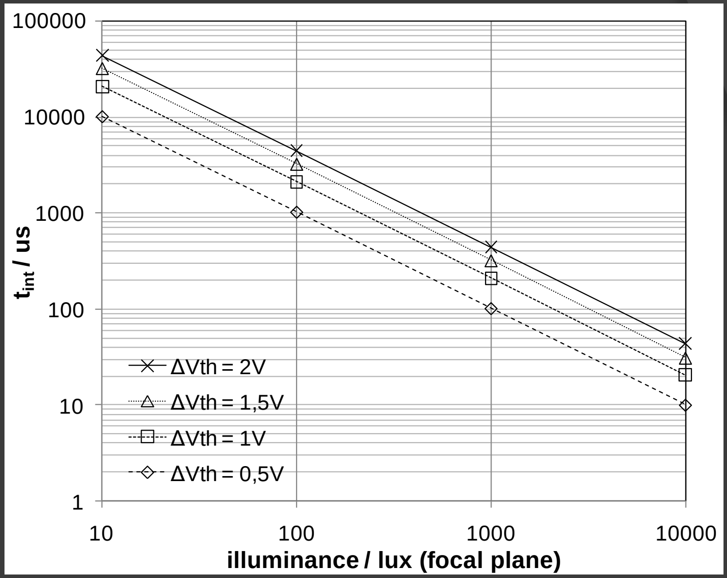


- **Photoreceptor:** logarithmic intensity → gain control mechanism that is sensitive to **temporal contrast = relative change**
- **Differencing amplifier** removes DC, amplifies pos/neg transients
- Two **threshold comparators** monitor ganglion output, spike generation
- Output: **asynchronous spike events** (circuit is **reset** after each event)

Lichtsteiner, P., Posch, C., Delbruck, T., "A 128 × 128 120dB 30mW asynchronous vision sensor that responds to relative intensity change," **ISSCC** 2006 (**JSSC** 2008)

Encoding Gray-Level Data in Time: PWM Imaging





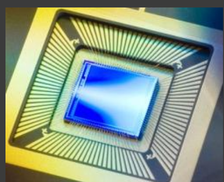
Measured **SNR** vs. **integration swing** $\boldsymbol{\Delta V_{th}}$ and light intensity:

SNR = **56dB** for $\boldsymbol{\Delta V_{th}}$**= 2V**/10Lx
(42.3dB for ΔV_{th}= 100mV/10Lx/2ms)
→ 9.3 Bit grayscale resolution

FPN < 0.25%

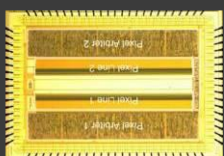
CMOS Neuromorphic Vision Sensors Gallery

Presented at:



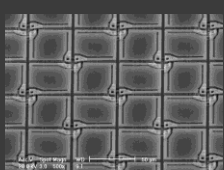
Tmpdiff128 – 128 × 128 pixel array sensor
high-dynamic-range, low-power temporal contrast dynamic vision sensor with in-pixel analog signal processing
ISSCC 2006, SSCS "Jan Van Vessem" Award, IEEE J. of Solid-State Circuits 2008

ISSCC



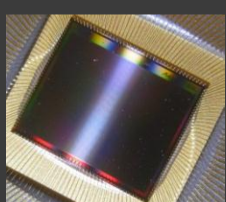
DLS – 2 × 256 pixel line sensor
dual-line optical transient sensor with on-chip precision time stamp generation and digital arbitration for high-speed vision
ISSCC 2007

ISSCC



DVS-IR – 64 × 64 pixel IR array sensor
transient vision sensor for the thermal infrared (IR) range with micro-machined bolometer IR detector technology
ISCAS 2008 "SSTC Best Paper Award", IEEE ICECS 2007 "Best Paper Award", IEEE Sensors Journal 2009

IEEE ISCAS

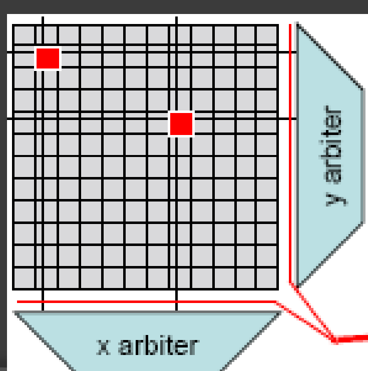


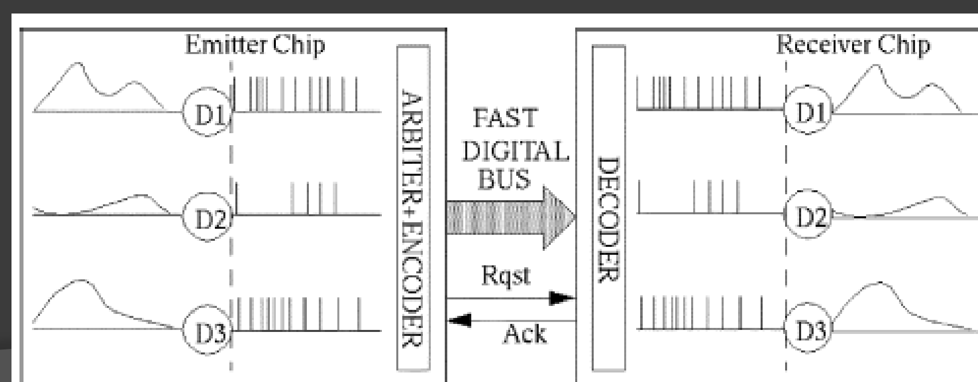
ATIS – QVGA event-driven dynamic vision and image sensor
QVGA ultra-wide dynamic range CMOS imager and dynamic vision sensor with focal-plane lossless video compression
ISSCC 2010, ISCAS 2009 "SSTC Best Paper Award", IEEE J. of Solid-State Circuits 2010 (invited)

ISSCC

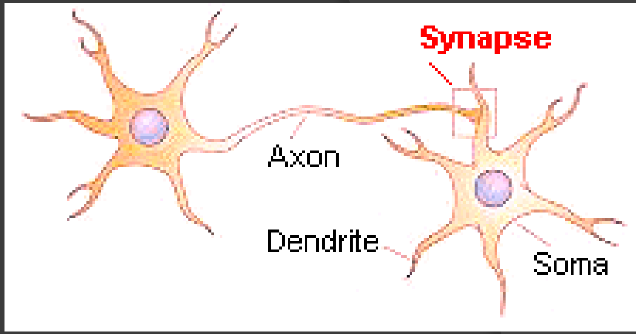
Wiring – address-event representation

- How to get the data off the array quickly?
- Mobility of electrons in silicon is about 10^7 times that of ions in solution,
- Signal transmission speed: lightspeed vs. few meters / sec
- Solution: **Softwiring**
- Each neuron is assigned an "address" → Address Event (AE)
- When neuron fires it pushes its address onto a **shared asynchronous** bus
- Asynchronous digital circuits map and route the address events to other nodes or different chips or (external) processing units





Processing and Storage



- N1 **spikes**—pulse travels down the axon to the synapse of target N2.
- The synapse of N2—having **stored its own state locally**—evaluates the importance of the information coming from N1 by integrating it with **own previous state** and **strength** of connection to N1
- **Two pieces of information**—signal from N1 and state of N2's synapse—**flow** toward body of N2
- When information reaches N2, there is only a **single value—all processing has already taken place during the information transfer**.
- Storage and processing happen at the ***same time*** and in the ***same place***.
- This **LOCALITY** is one of main reasons for **energy efficiency** of biological brains