Cryogenic Electronics for Very Large Liquid Argon Neutrino and Nucleon Decay Detectors

Veljko Radeka
BNL

Acknowledgements:

BNL: G. De Geronimo, S. Li, H. Chen, C. Thorn, B. Yu, A. D'Andragora, S. Rescia
FNAL: G. Deptuch, R. Yarema
Georgia Tech: J. Cressler

TWEPP 2011, Vienna, Sept. 26-30

Outline:

1. Solar neutrino deficit and neutrino oscillations
2. Giant Lar facility dreams and plans
3. TPC and signal formation
4. Giant TPCs readout challenge and essential block diagram
5. CMOS properties vs temperature
6. CMOS lifetime and electronics reliability
7. ASIC design
8. ASIC results
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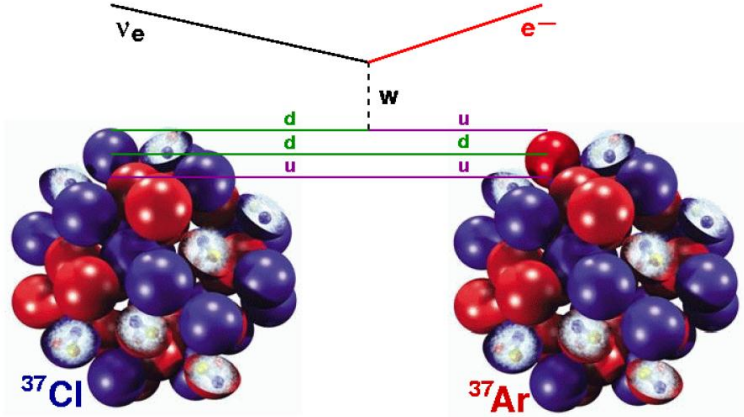
1968--Ray Davis starts a fight that lasts 30 years

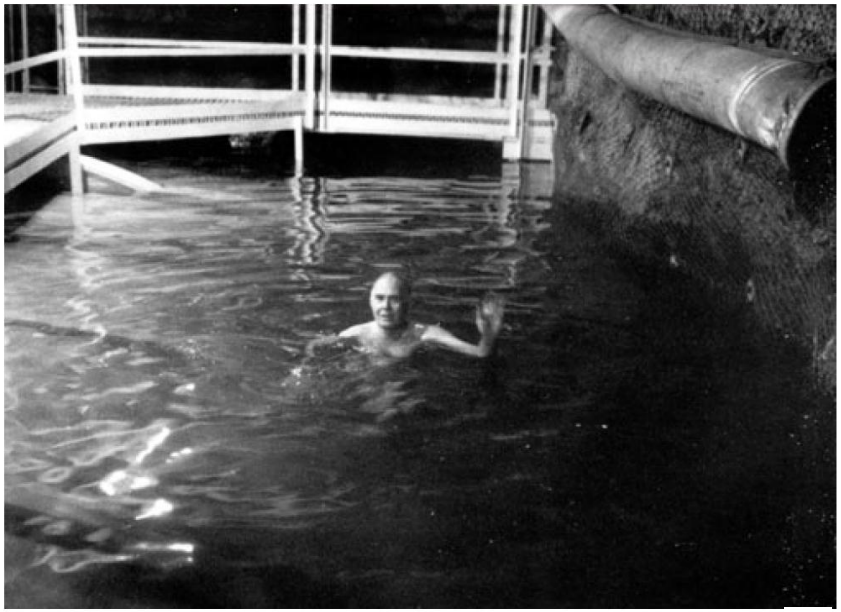
- Used a large vat of dry cleaning solution to look for Argon from inverse beta decay



36 Ar atoms per month.

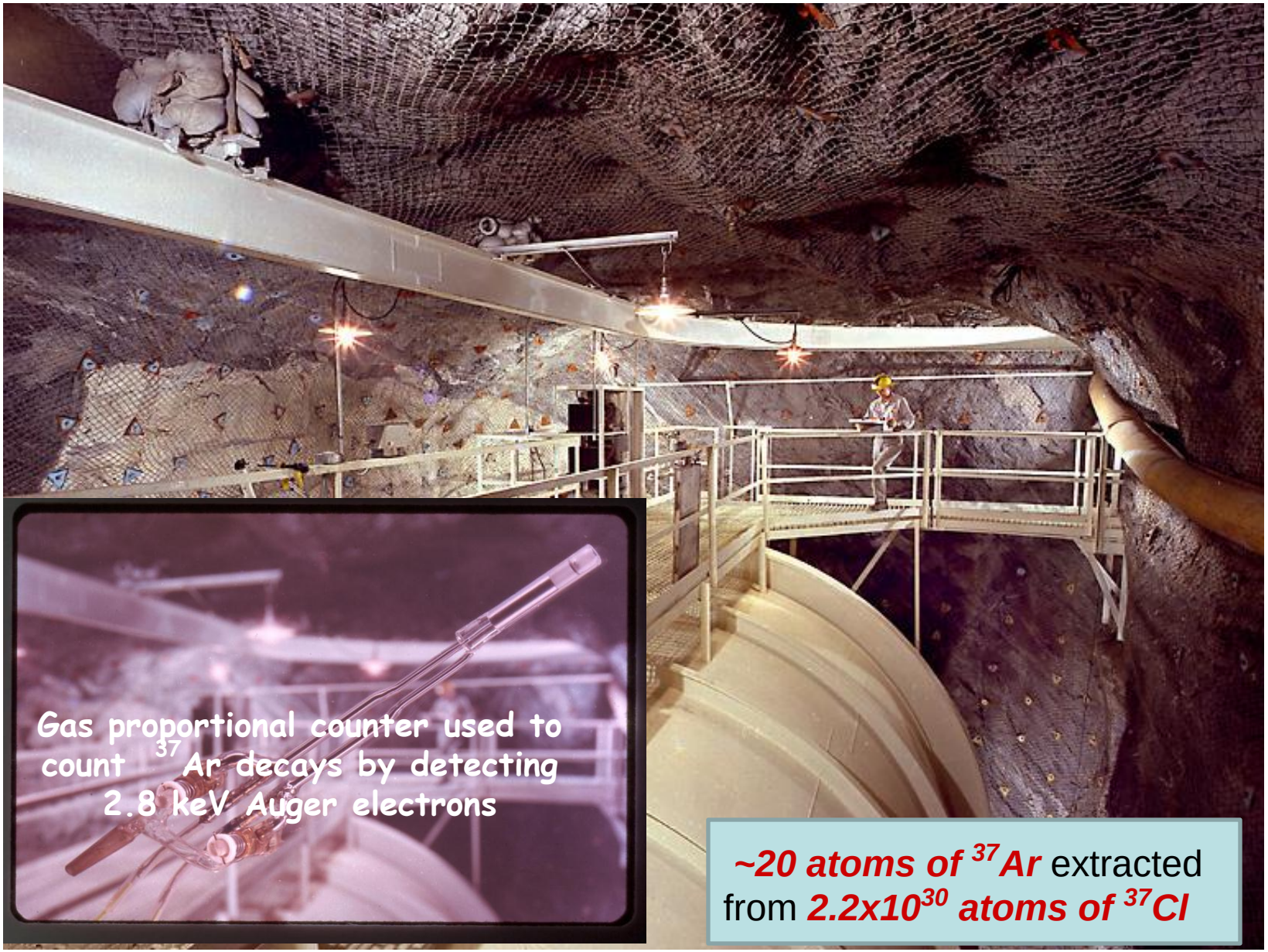
$$\frac{\phi_{\nu_e}(\text{Homestake})}{\phi_{\nu_e}(\text{Theory})} = 0.34 \pm 0.06$$

- Remained mired in controversy for 30 years. Do we understand fusion? Is the experiment correct? Could it be new physics, e.g. Pontecorvo's oscillations?



Ray Davis

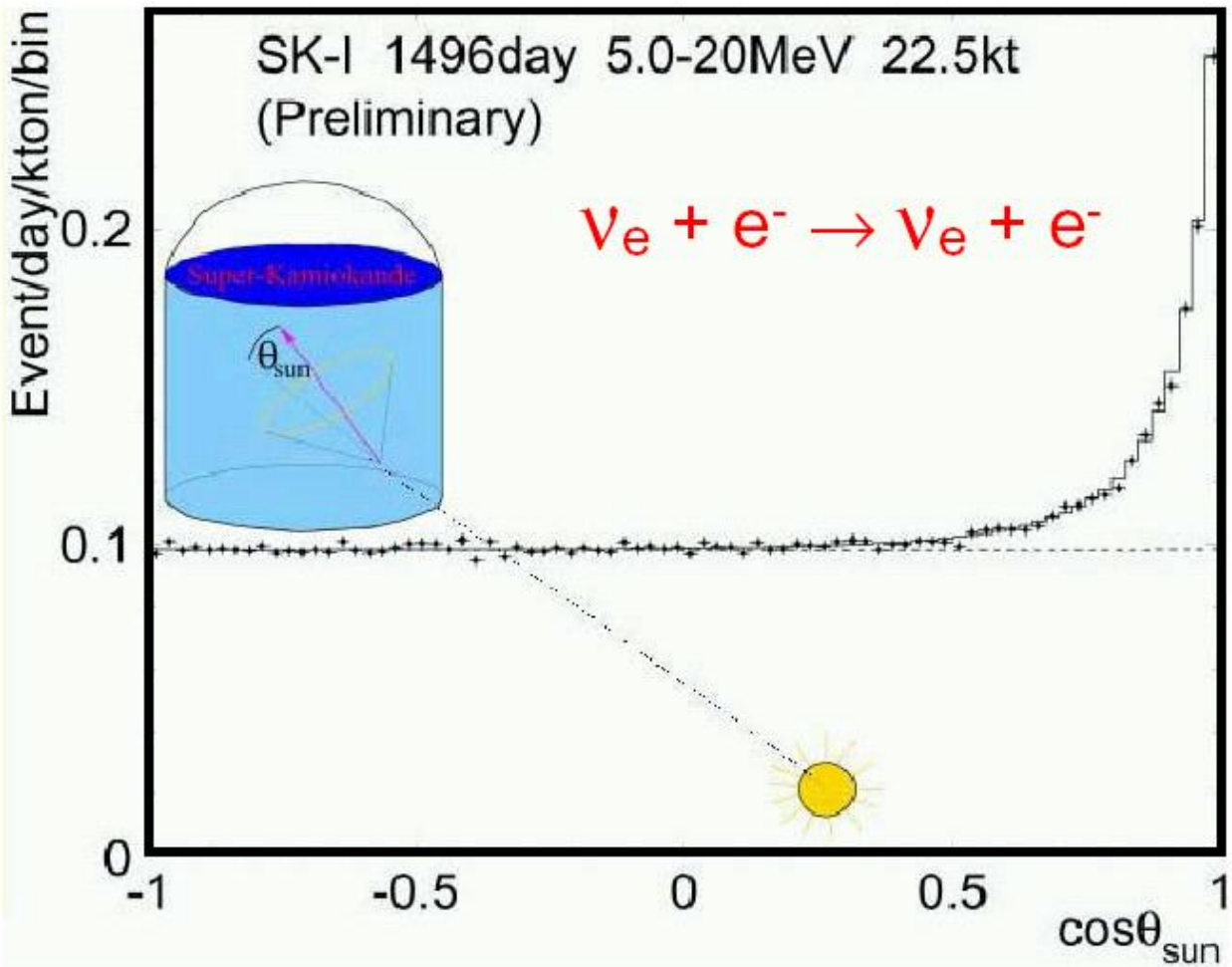
The C_2Cl_4 Tank (~400m^3) - Homestake exp., 1478m below the surface



Neutrinos and the Sun

- The source of the Sun's energy is fusion of 4 hydrogen atoms to make a helium atom
- Each time this reaction occurs, 2 (electron) neutrinos (ν) are released
- 1.8×10^{39} neutrinos per second come from the center of the sun and here on Earth, ~100 billion pass through your fingernail (1 cm^2) every second
- For an average size person, an atom in the body will capture a neutrino every 70 years
- *Davis' result (relative to the Standard Solar Model prediction): ~**1/3***
- *This was the only experiment for over two decades searching for solar neutrinos. **It opened up a new field of particle and astrophysics** …*

Super-Kamiokande solar neutrino result



from M. Smy (ν2002)

Resolution of Solar ν Deficit (2002)

SNO – Sudbury: Deep Underground: 6,000 mwe
Heavy water (D_2O)

Detect ν_e :	charged current	(CC)
	elastic scatter	(ES)
Also ν_μ, ν_τ :	neutral current	(NC)
ν_e	$n \rightarrow e^- p$	CC
ν_e	$e^- \rightarrow \nu_e e$	ES
$\left\{ \begin{matrix} \nu_e \\ \nu_\mu \\ \nu_\tau \end{matrix} \right\} d \rightarrow \left\{ \begin{matrix} \nu_e \\ \nu_\mu \\ \nu_\tau \end{matrix} \right\} d$		NC

Result : **~1/3 ν_e**
~ 2/3 ($\nu_\mu + \nu_\tau$) ⇒ *Neutrino oscillations*

Total flux agrees with that expected from the sun (predicted by J. Bahcall 3 decades earlier)

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2. **Giant facility plans (and dreams!) - to study neutrino oscillations, nucleon decay, supernova neutrinos …**
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Beam: 700 kW, 60-120 GeV, 5 years ν + 5 years $\bar{\nu}$
on-axis, wide band, upgradable to 2.3 MW

Baseline: 1300 km FNAL to Homestake

Far Site: Underground location to facilitate broad program

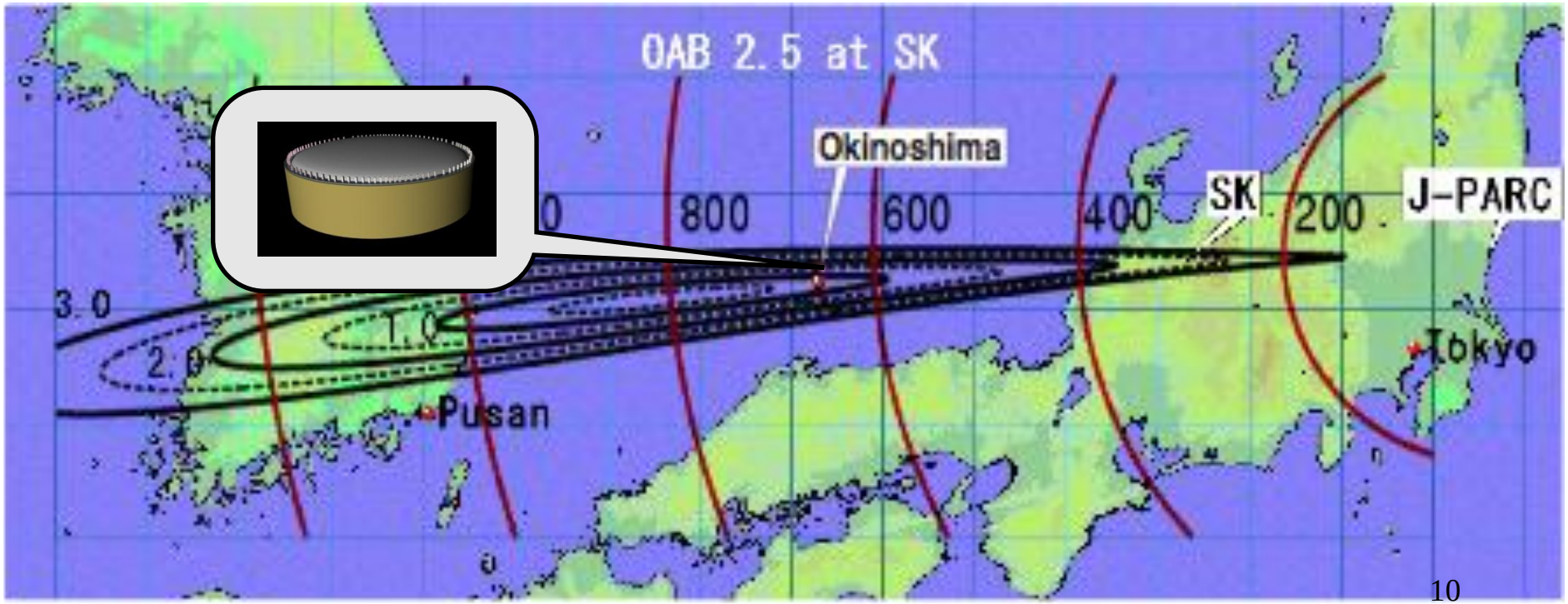
Near Site: on current Fermilab property

Configurations: several options under study for beam, near, and far detectors

J-PARC to Okinoshima

arXiv:0804.2111

Distance = 658 km
Off-axis angle = 0.76º (2.5º @ SK)
100 kton liquid Argon



→ **Good coverage of 1st & 2nd oscillation maximum**

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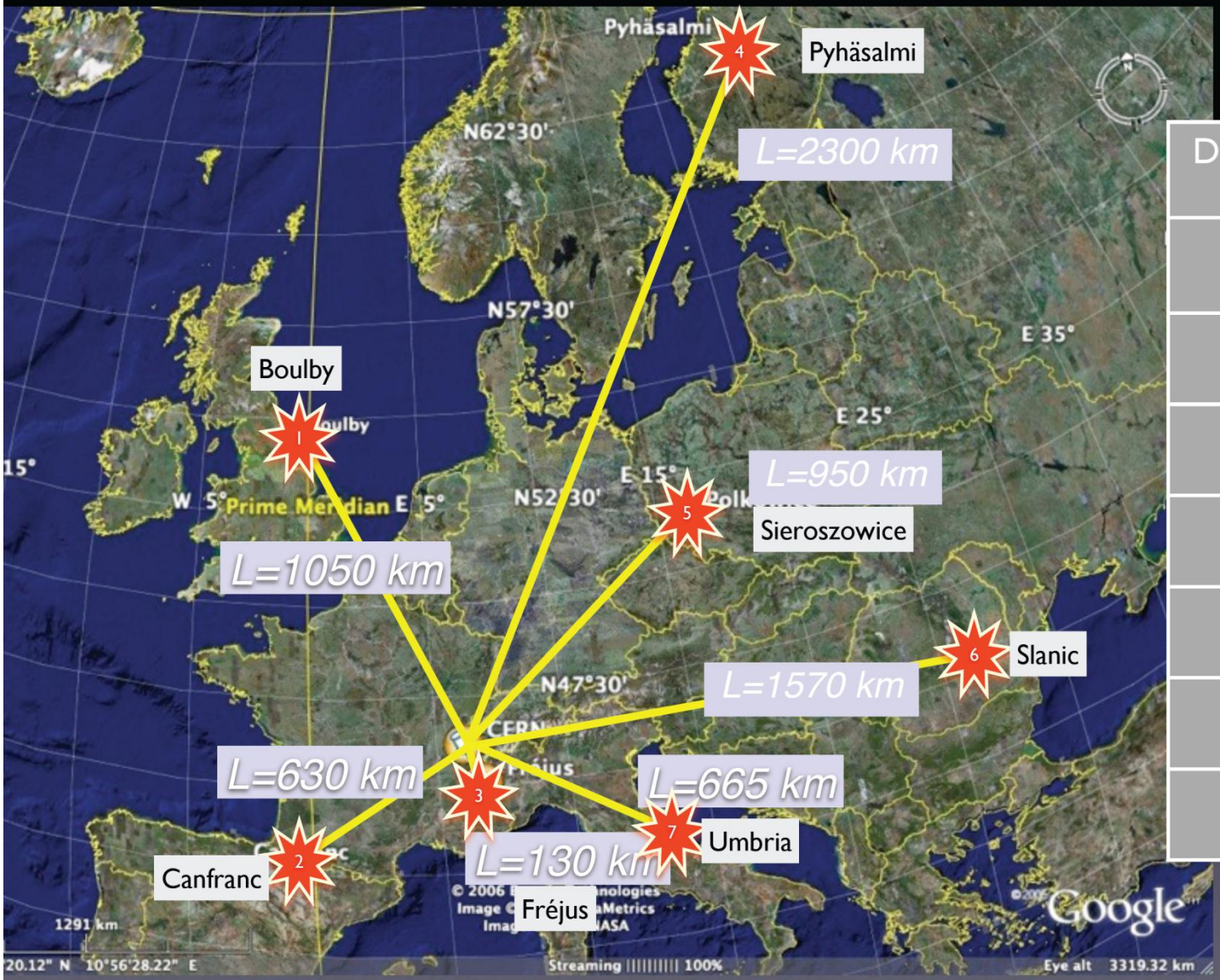
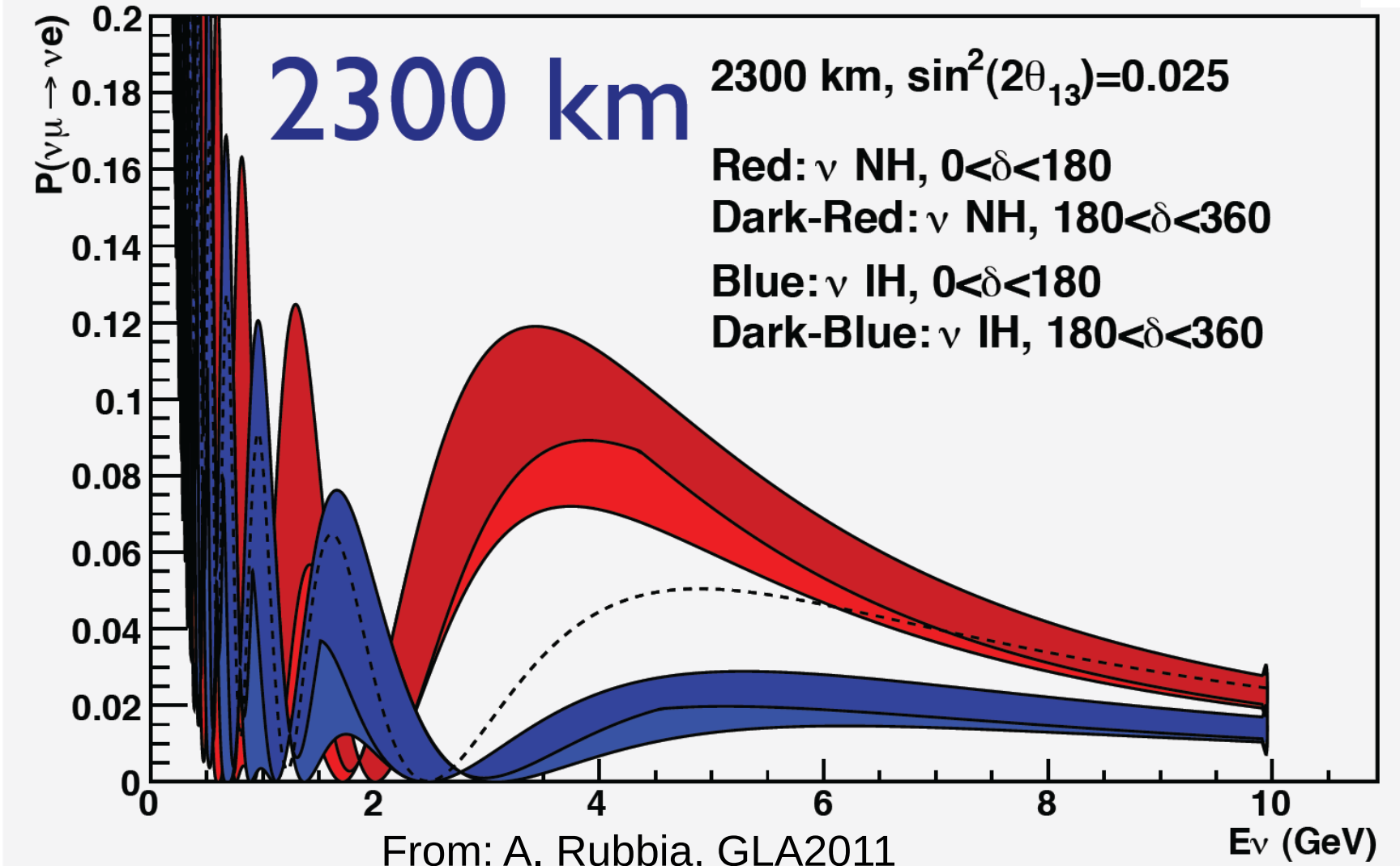
Various baselines possible



Distance/ km	1st oscillation
130	0.26
630	1.27
665	1.34
950	1.92
1050	2.12
1570	3.18
2300	4.65

Probability of neutrino oscillations vs neutrino energy



From: A. Rubbia, GLA2011

Cosmic Ray experiment EMMA at shallow depth

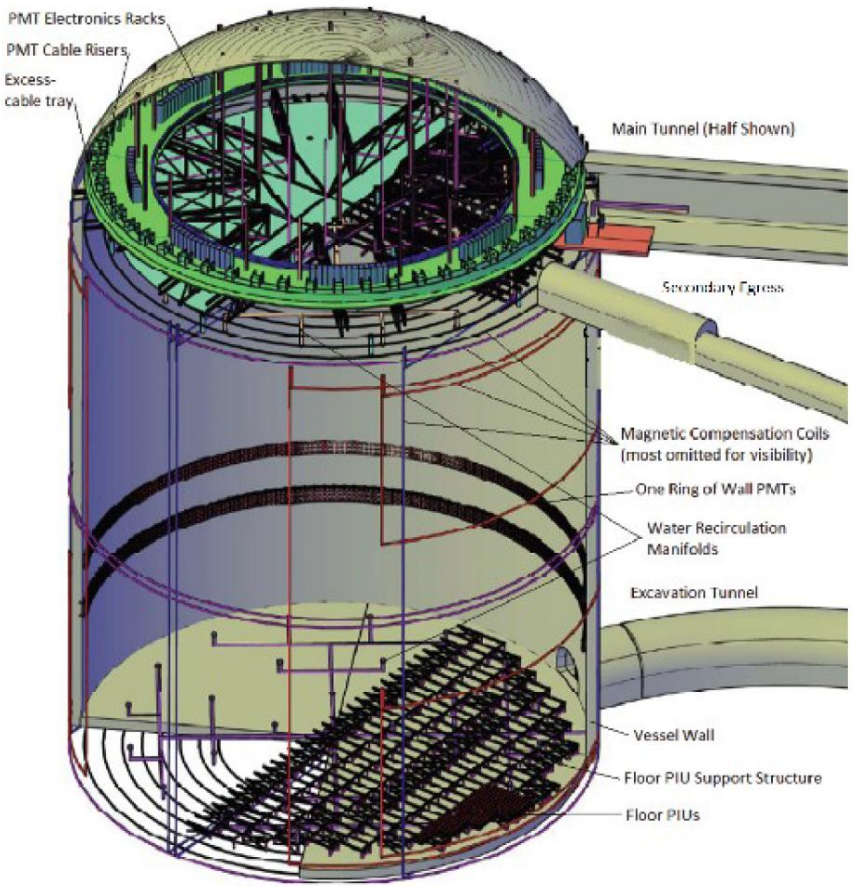
250 m long tunnel and a cavern at 1400m excavated for LAGUNA R&D

Cafeteria, meeting room and sauna at 1400 m below ground

Mobile phones work and internet available also at 1400 m

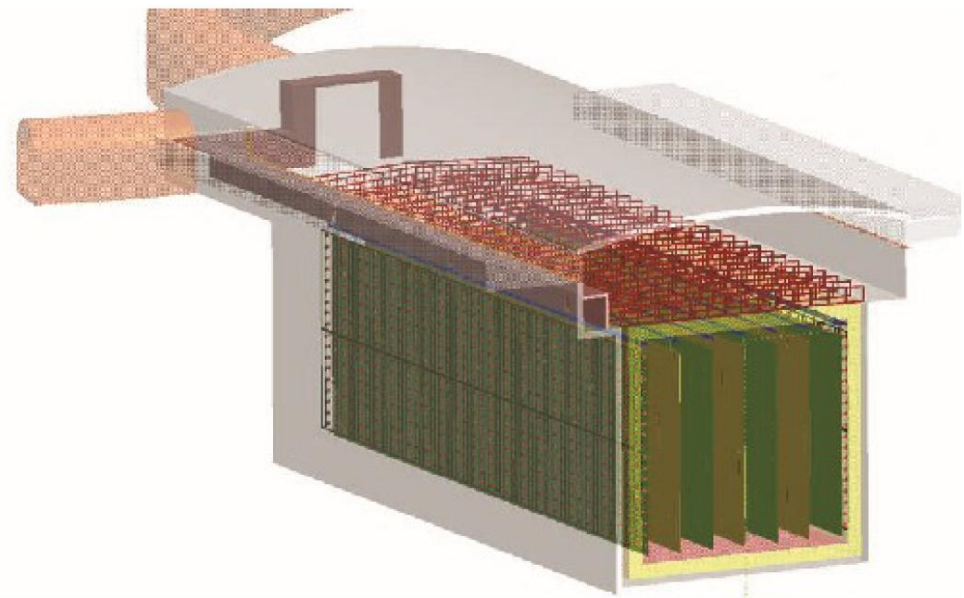
OVERVIEW: Two Far Detector Options for **LBNE**

200 kT water Cherenkov



One 200 kT fiducial WC detector
Located at the **4850 foot level**

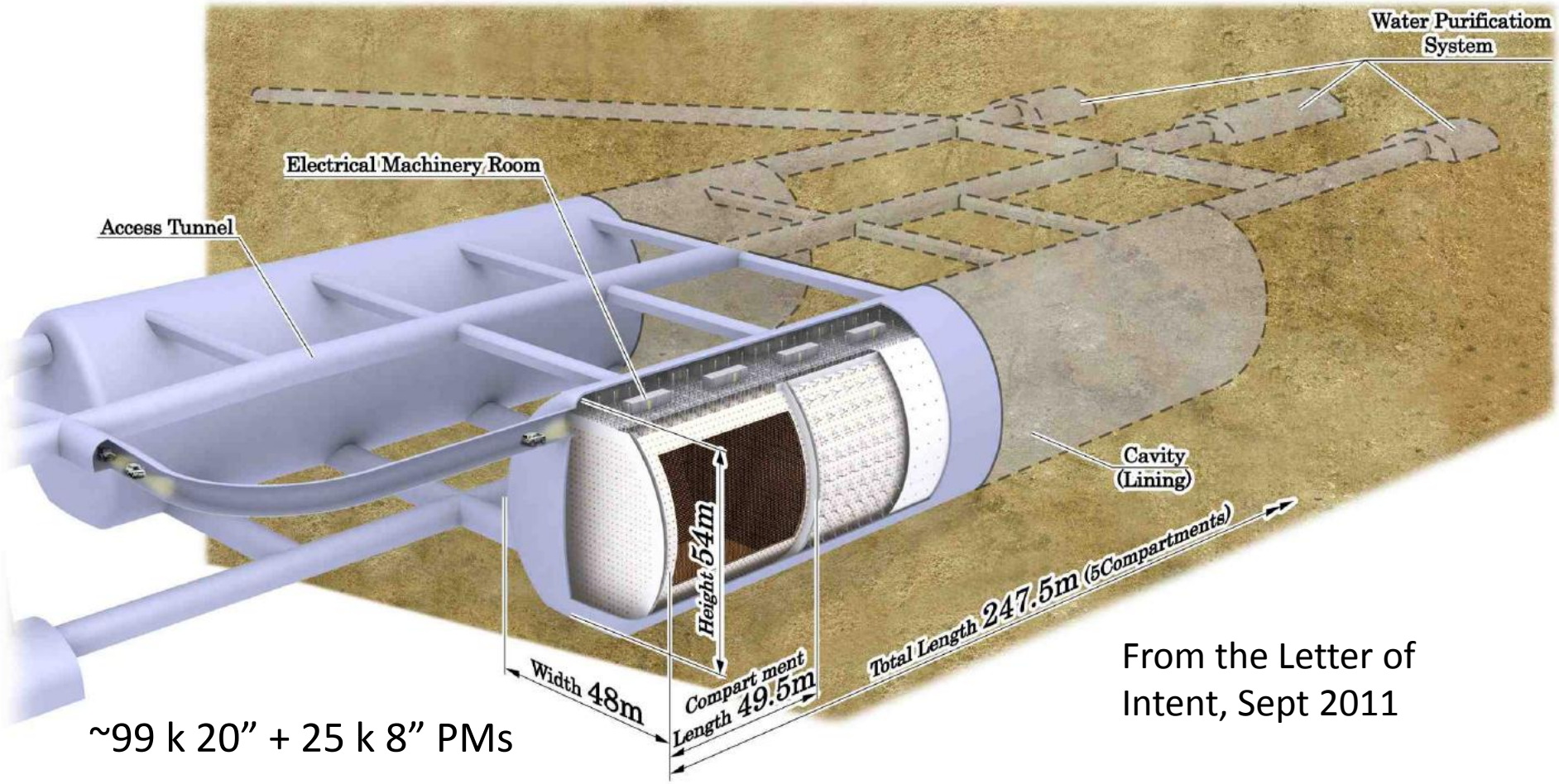
34 kT liquid argon



Two 17 kT fiducial LAr detectors
To be located at a new drive-in site at **800 foot level**. (one detector shown here)

Hyper-K (~20xS-K)

Total (fiducial) vol. ~0.99(0.56) Mton H_2O

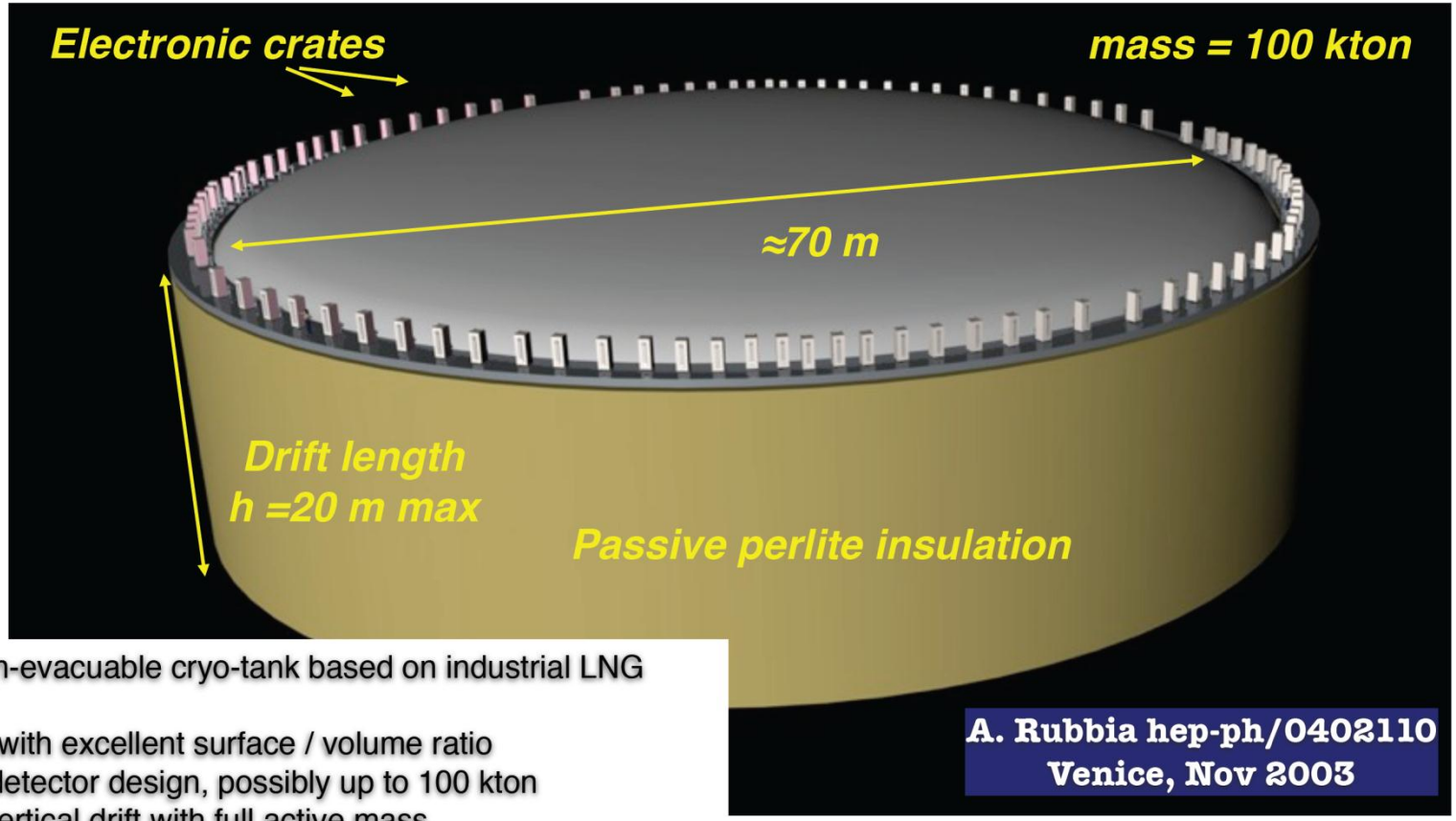


~99 k 20” + 25 k 8” PMs

From the Letter of Intent, Sept 2011

Giant Liquid Argon Charge Imaging ExpeRiment

A scalable detector with a non-evacuable dewar and ionization charge detection with amplification



- Single module non-evacuable cryo-tank based on industrial LNG technology
- Cylindrical shape with excellent surface / volume ratio
- Simple, scalable detector design, possibly up to 100 kton
- Single very long vertical drift with full active mass
- Double phase, large area LAr LEM-TPC for long drift paths
- Possibly immersed visible light readout for Cerenkov imaging
- Possibly immersed (high Tc) superconducting solenoid to obtain magnetized detector
- Reasonable excavation requirements (<250'000 m³)

We have developed an R&D roadmap to address this design→ pto

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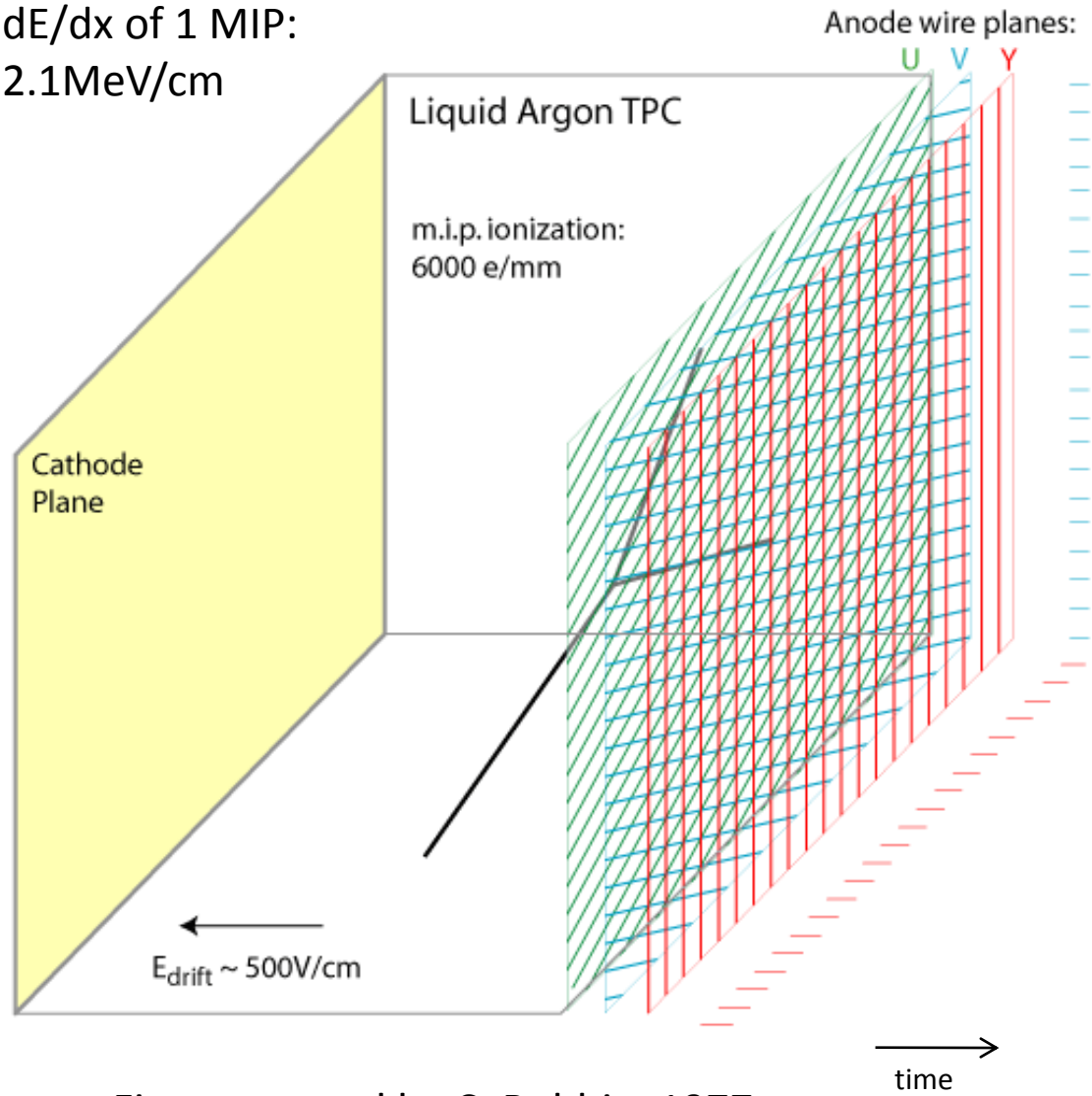
How Does a LArTPC Work

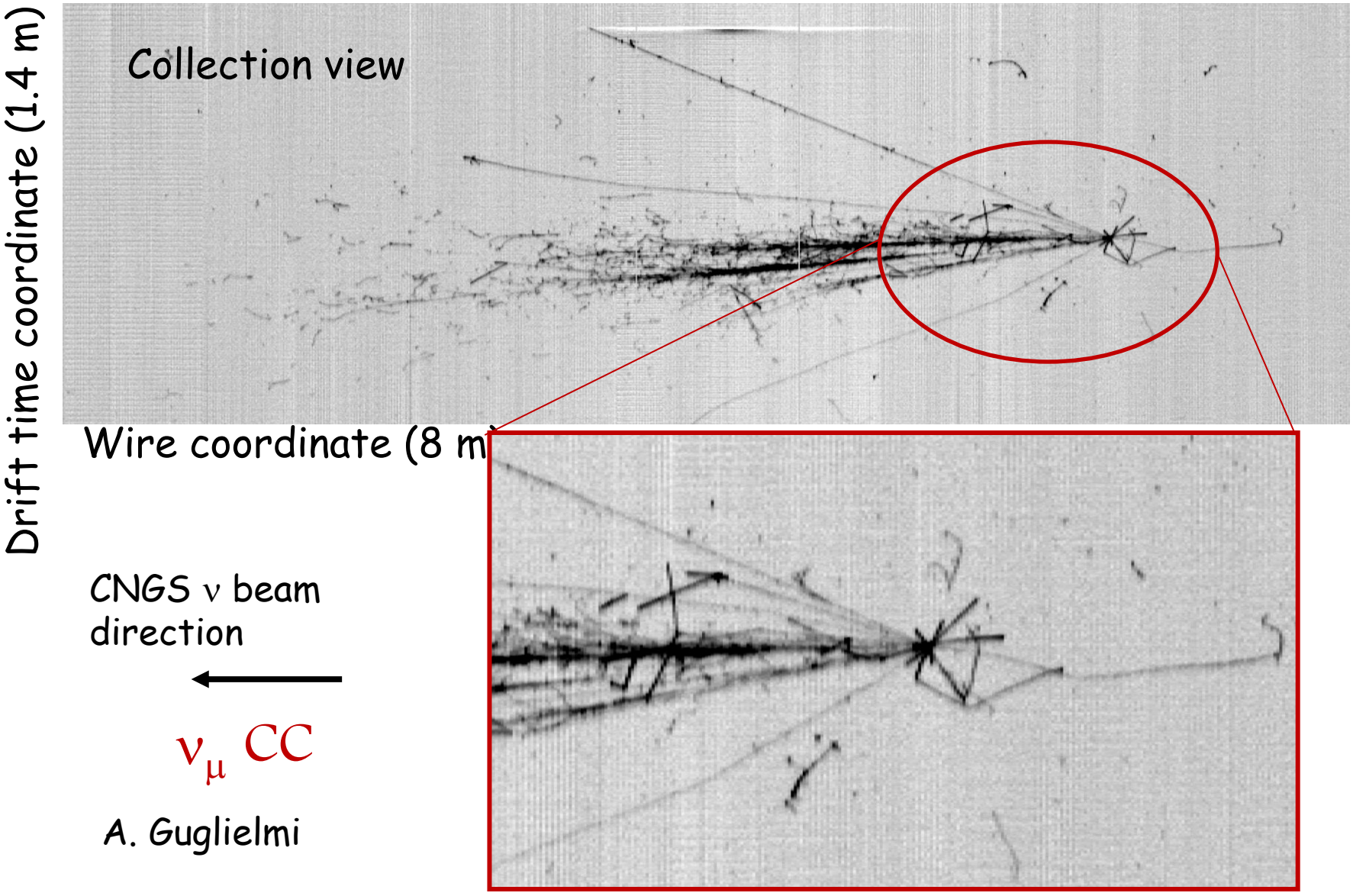
dE/dx of 1 MIP:
2.1MeV/cm



First proposed by C. Rubbia, 1977

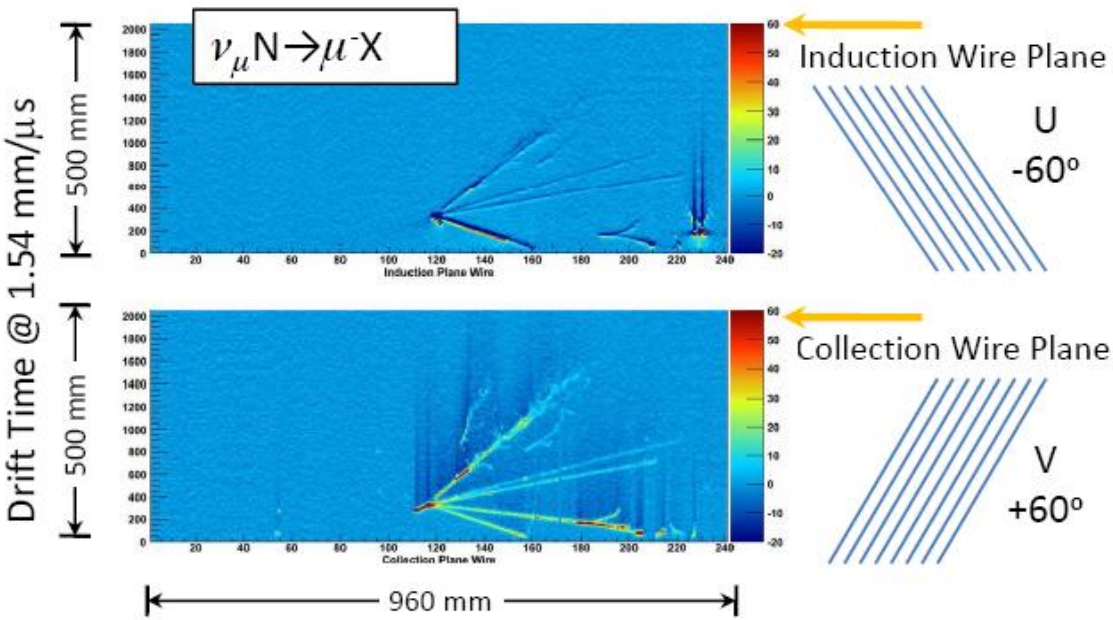
- Sense (anode) wires (up to ~ 10m long):
  ~14-**31 kwires/kton**
  - up to **200 pF/wire**
  - collecting (Y)
  - non-collecting (U,V)
- charge sensitivity
  - range ~300 fC
  - ENC < 1,000 e^-
- sample/buffer events
  - ADC 10-12-bit, 1-2 MS/s
  - **3,000 deep buffer**
- **digital multiplexing**
  - **128:1** to1024:1 two-three stages
  - **power constraint**
  - **~ 10 mW** /wire
- operation in LAr
  - **> 30 years**

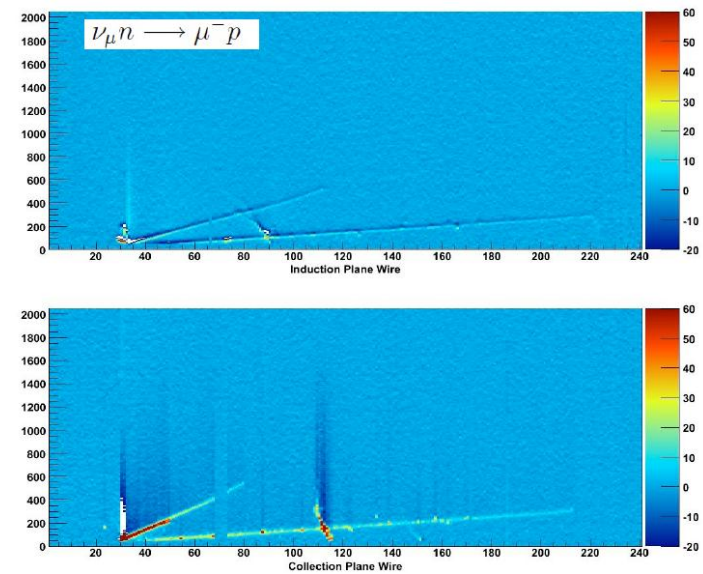
First CNGS neutrino interaction in ICARUS T600



Advantages of LAr TPCs

Neutrino interactions recorded in the small LAr TPC at FNAL: ArgoNeut





- Full 3D event reconstruction
  sub-mm position resolution
- dE/dx for particle ID
  e/γ separation >90%
- Low energy threshold <5 MeV
- Scalable to multi-kiloton size

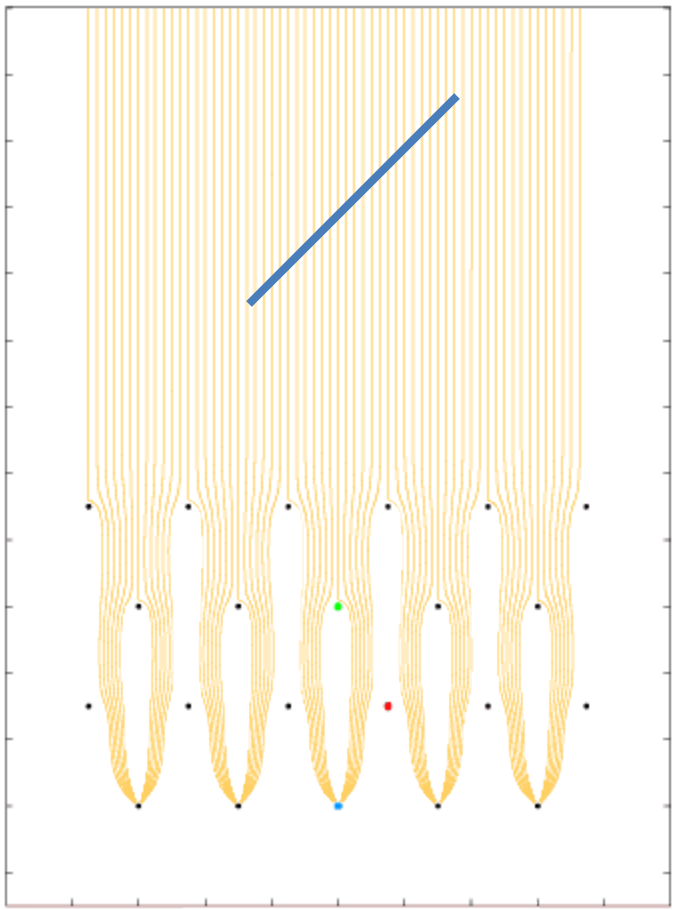
Optimized TPC geometry

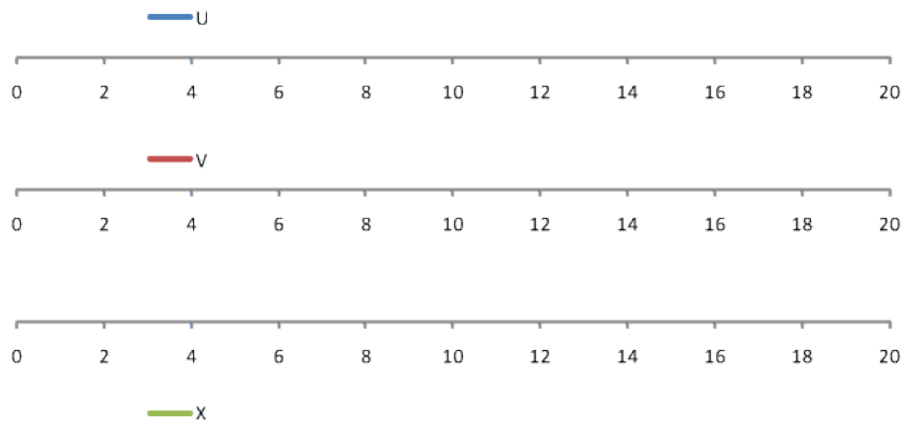
Low noise electronics

Multiplexed readout

High LAr purity

Signal Formation: Induced Signals from a Track Segment





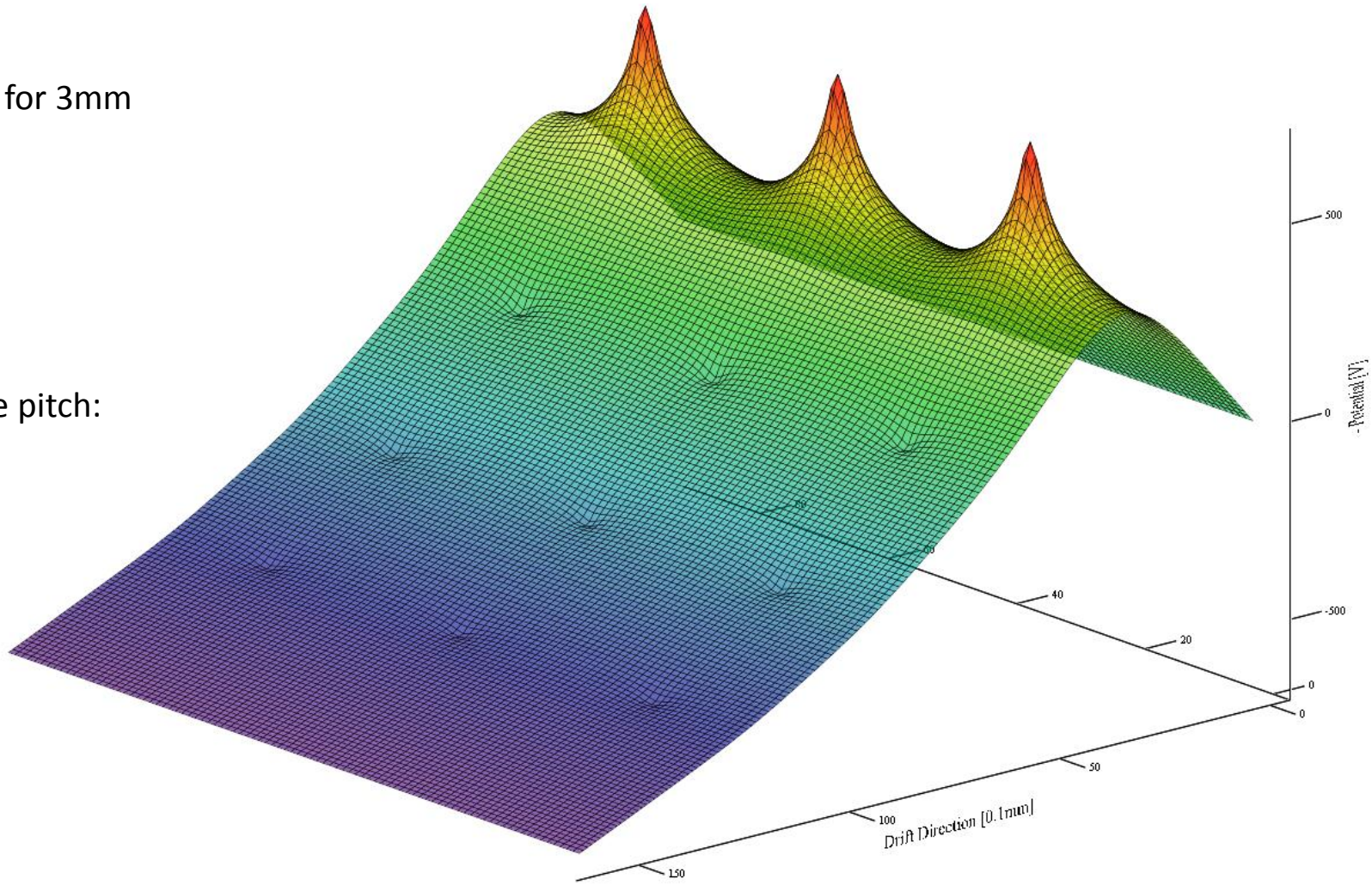
[μs]

LBNE style wire arrangement: 3 instrumented wire planes + 1 grid plane
Raw current waveforms convolved with a 0.5μs gaussian (~1/2 drift length) to mimic diffusion

Potential Distribution Near the Wires

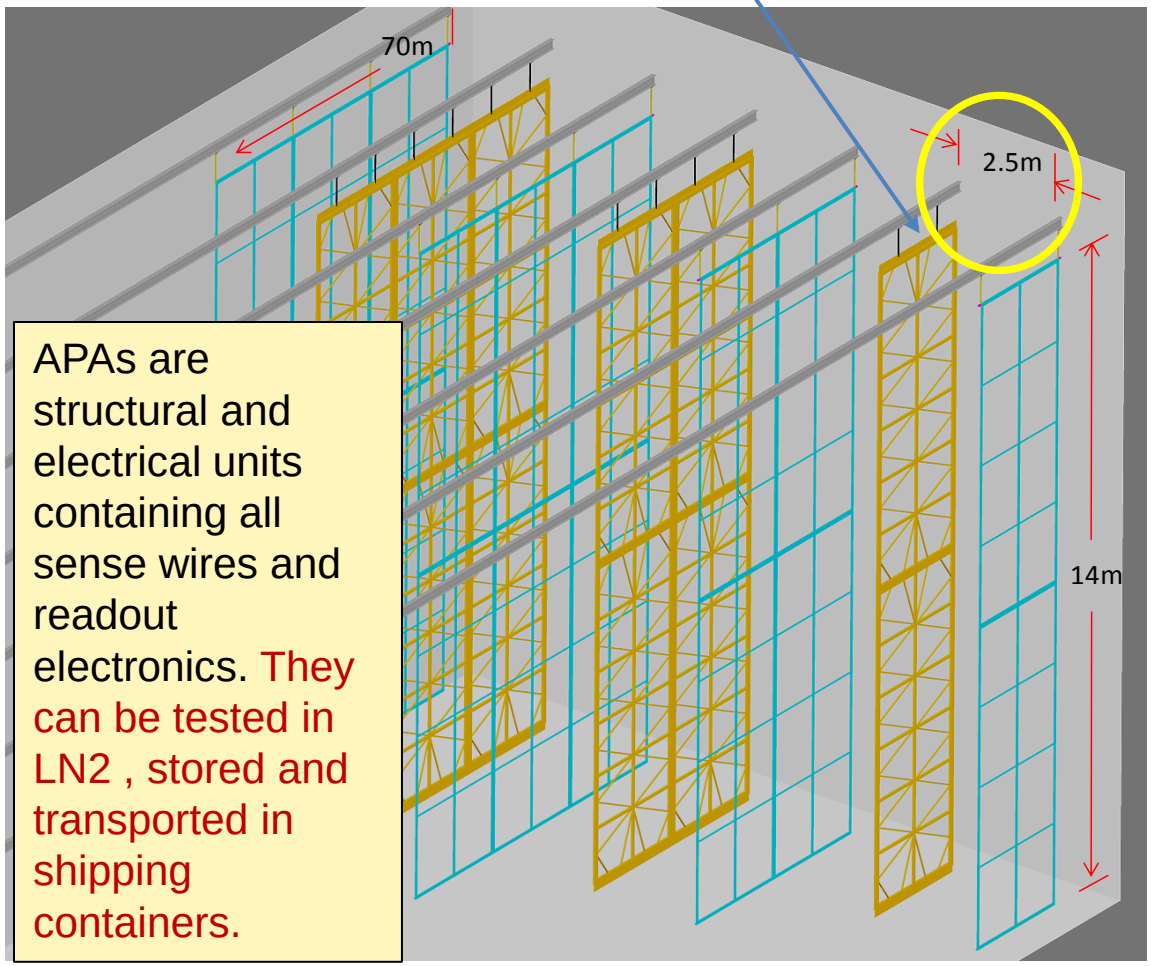
Bias Voltages for 3mm pitch:
V_G = -480V
V_U = -280V
V_V = 0
V_X = +700V

For 5mm wire pitch:
V_G = -690V
V_U = -385V
V_V = 0
V_X = +900V

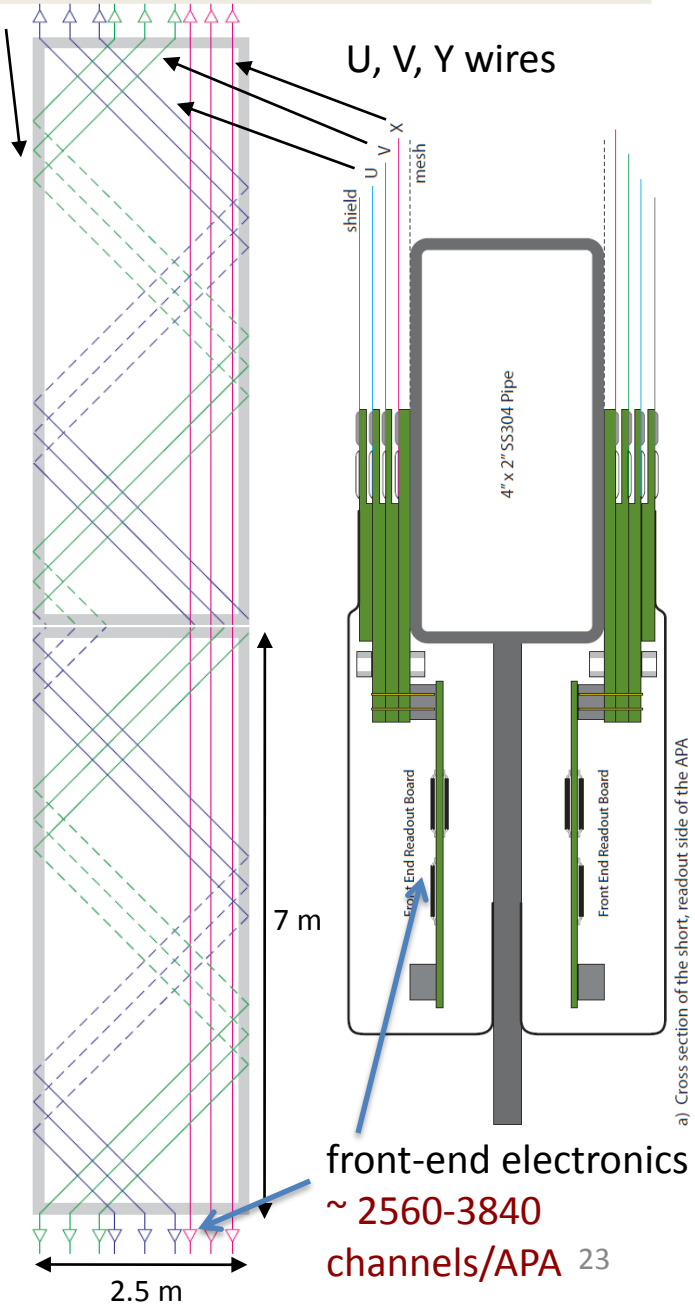


Anode Plane Assembly (APA) → modular TPC in a large cryostat

~5 APAs/kton, ~4.5mm wire pitch, 3.8m drift , 2560 wires/APA

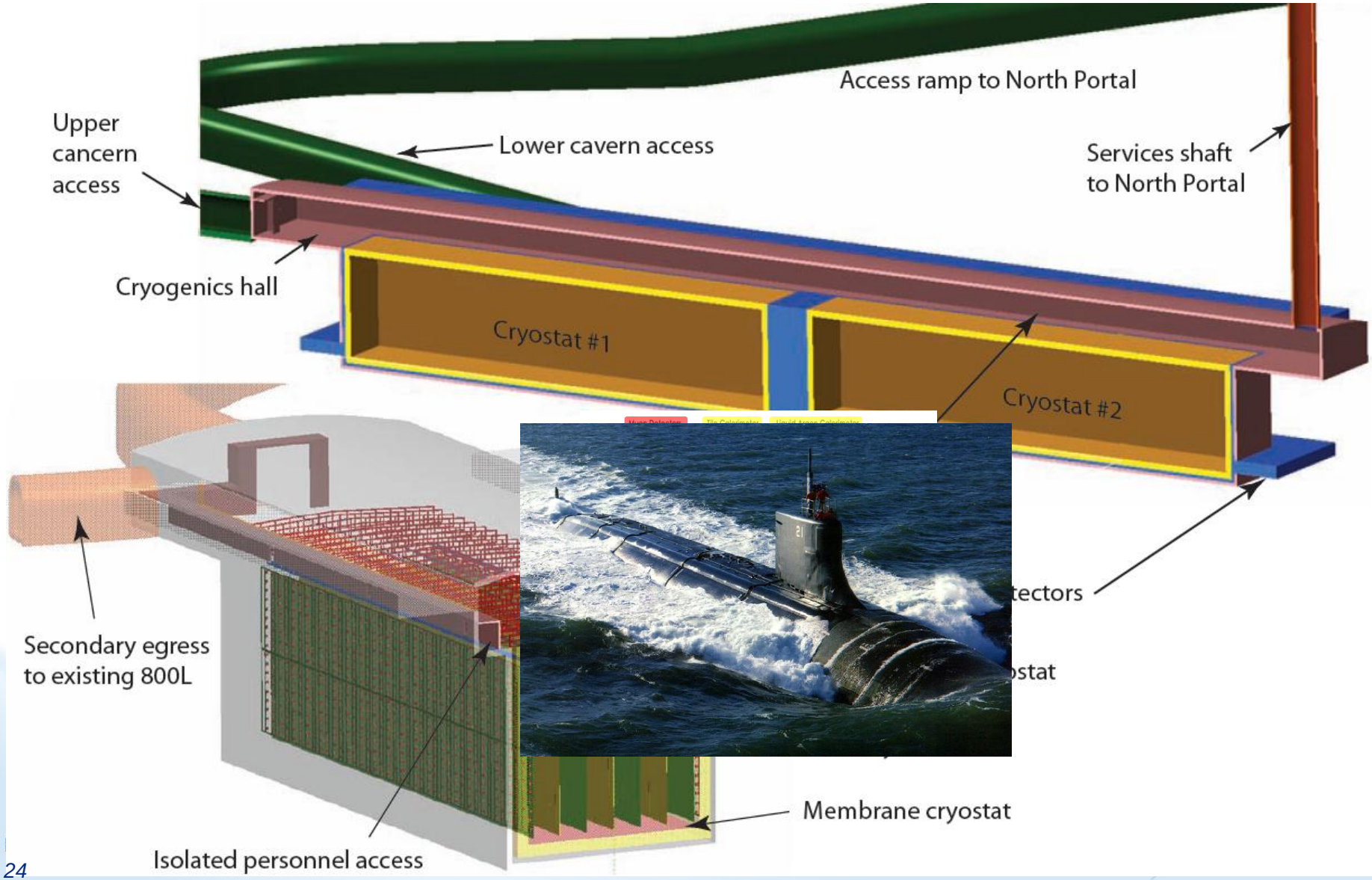


APAs are structural and electrical units containing all sense wires and readout electronics. They can be tested in LN2 , stored and transported in shipping containers.



front-end electronics ~ 2560-3840 channels/APA

LAr40 Conceptual Design at 800L



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ICARUS 600 ton LAr TPC (pioneered by C. Rubbia)

Front-end Electronics and DAQ

54000 channels

Liquid argon

Gas

Sense wires
(4-9m, 20pF/m)

Twisted pair cables
(~5m, 50pF/m)

H.V. (±300 V)

Decoupling
Boards (32 ch.)

(18 board + 1 CPU)/VME crate

Front-end
amplifiers
(32/board);
1500 e.n.c.

4 Multiplexers
(400ns x 8ch.)

FADC

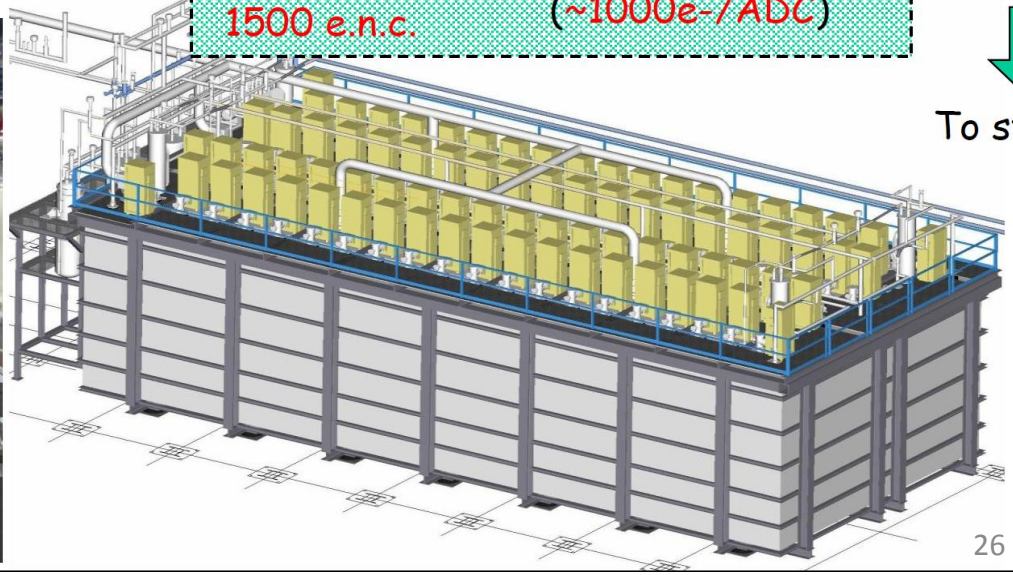
10bit FADC
400ns sampling
1mV/ADC
(~1000e-/ADC)

Multi-event
circular
buffer
(8x1ms)

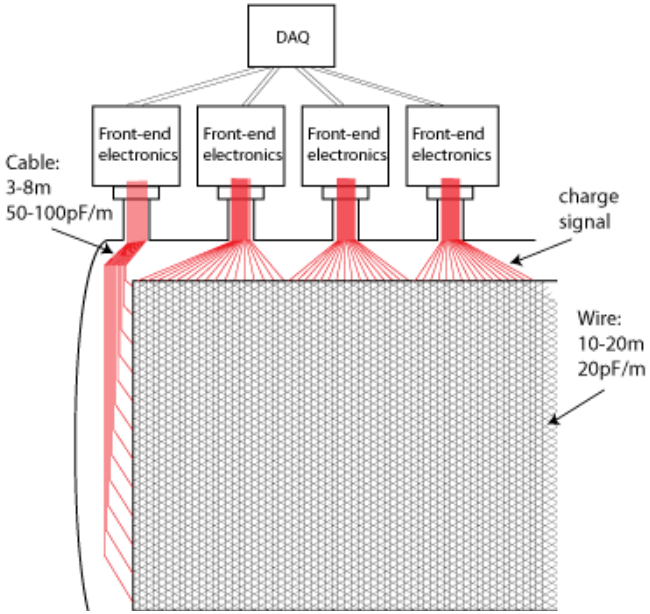
Time

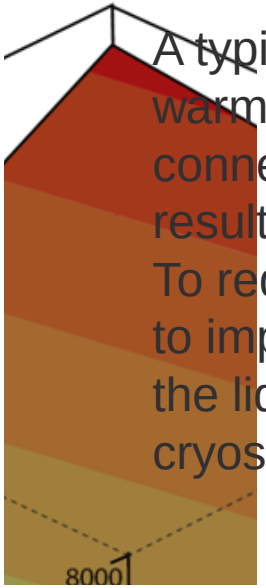
Continuous
waveform
Recording

To storage

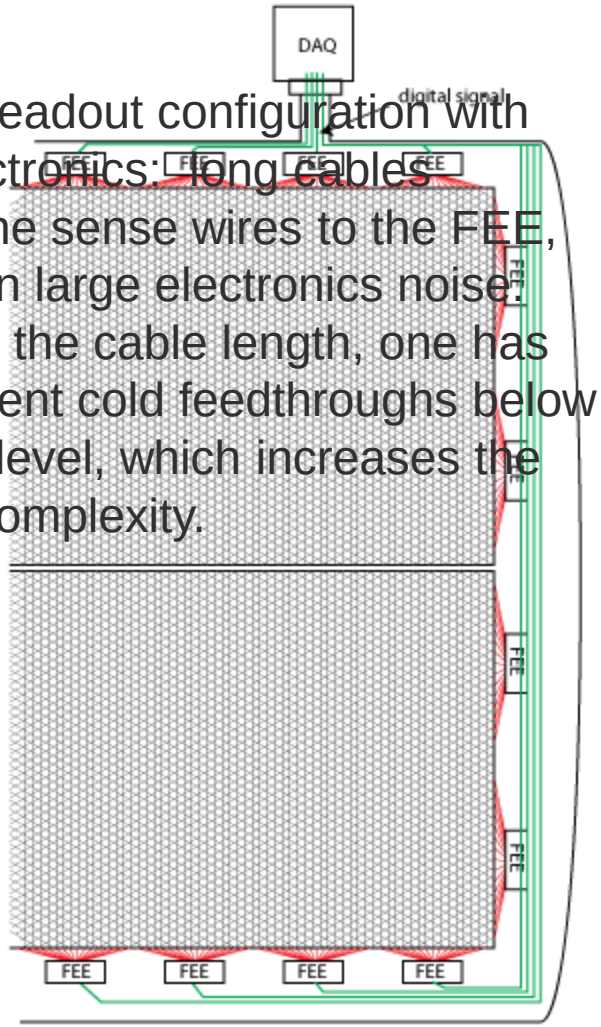


Key Technology in Building Large Scale LArTPC: Cold Electronics





A typical readout configuration with warm electronics: long cables connect the sense wires to the FEE, resulting in large electronics noise. To reduce the cable length, one has to implement cold feedthroughs below the liquid level, which increases the cryostat complexity.



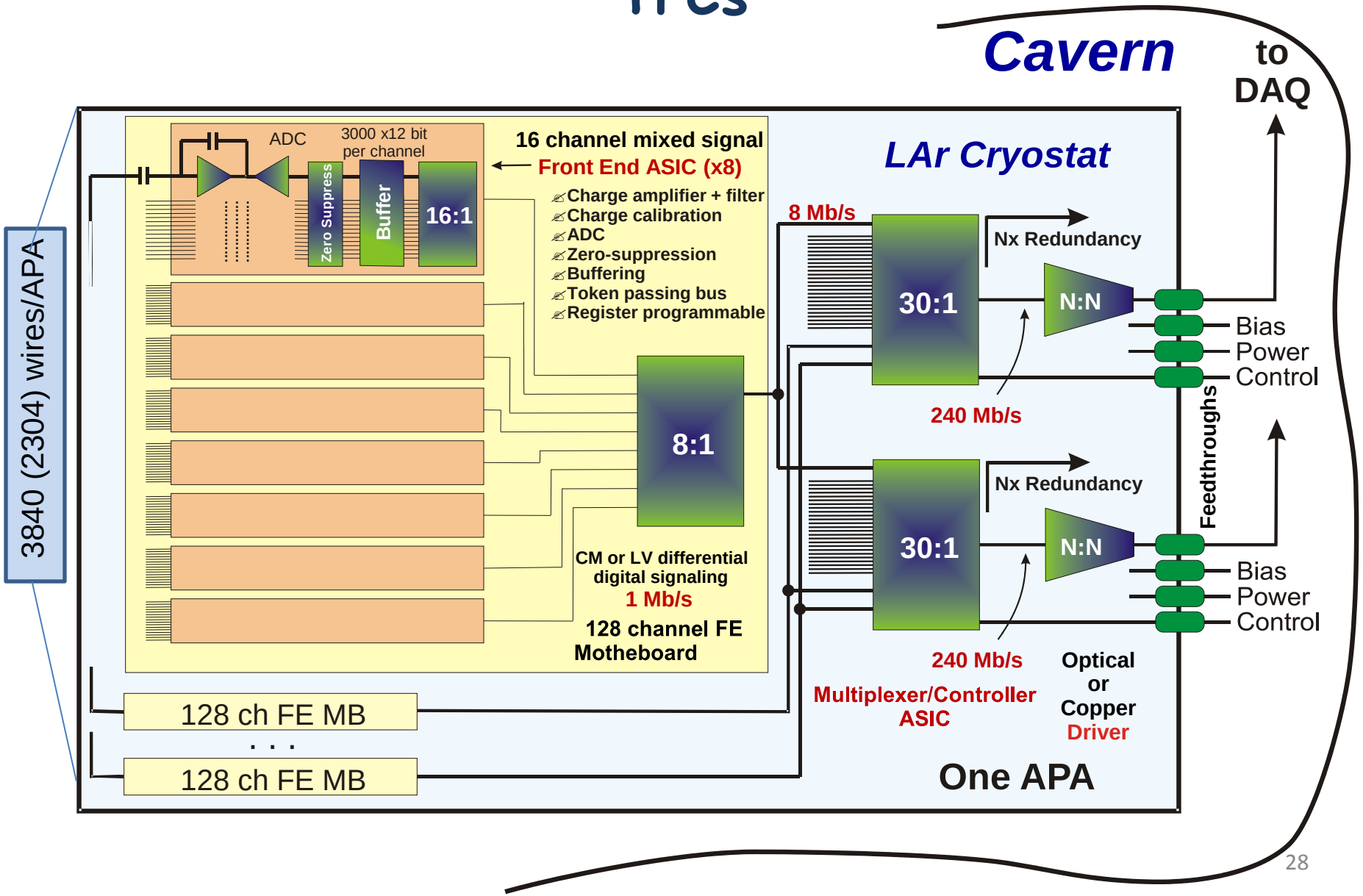
Stacked detectors for large cryostats

Having front-end electronics in the cryostat, close to the wire electrodes yields the best SNR

Highly multiplexed circuits with fewer digital output lines not only greatly reduce the number of cryostat penetrations, but also give the designers of both the TPC and the cryostat the freedom to choose the optimum configurations

Noise (ENC) *vs* Sense Wire and Signal Cable Length - in relation to MIP Signal for 3x3 and 5x5 mm Wire Spacing

Readout Electronics Outline for very large TPCs



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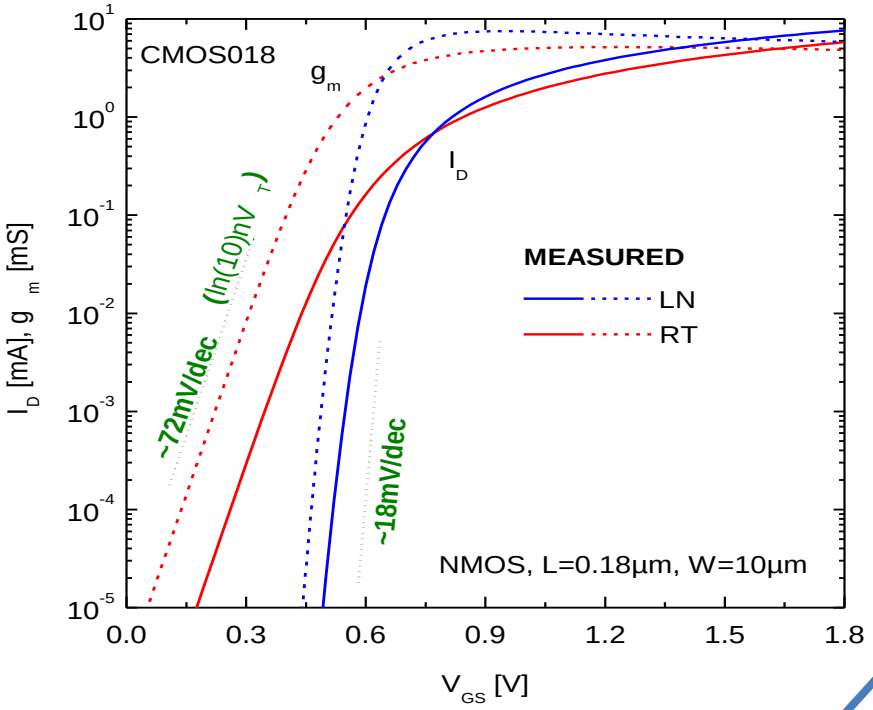
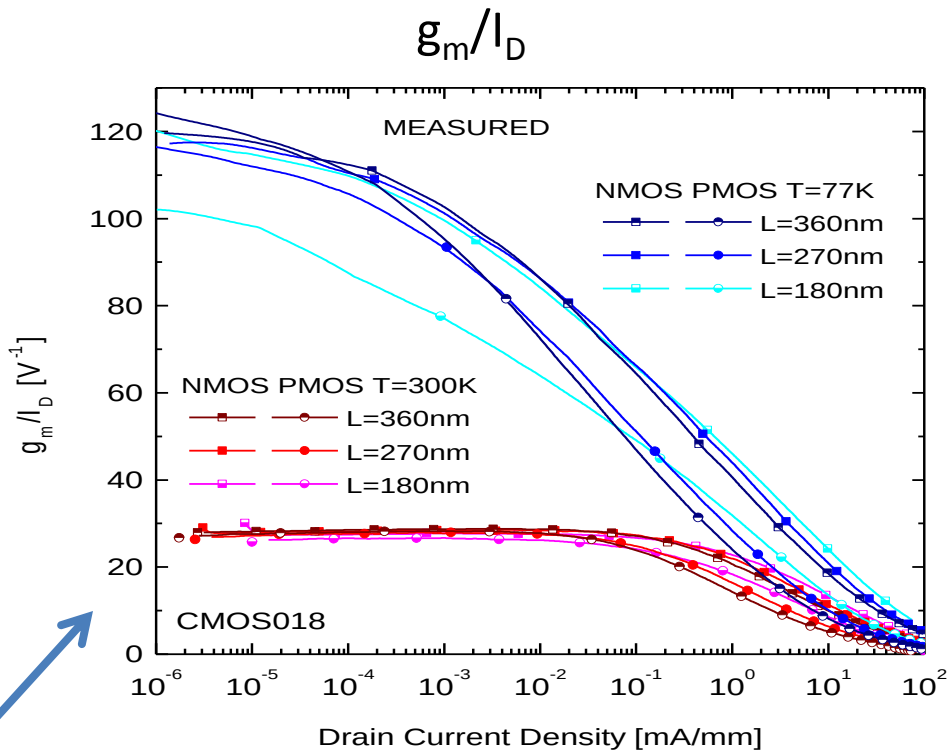
CMOS static characteristics vs T



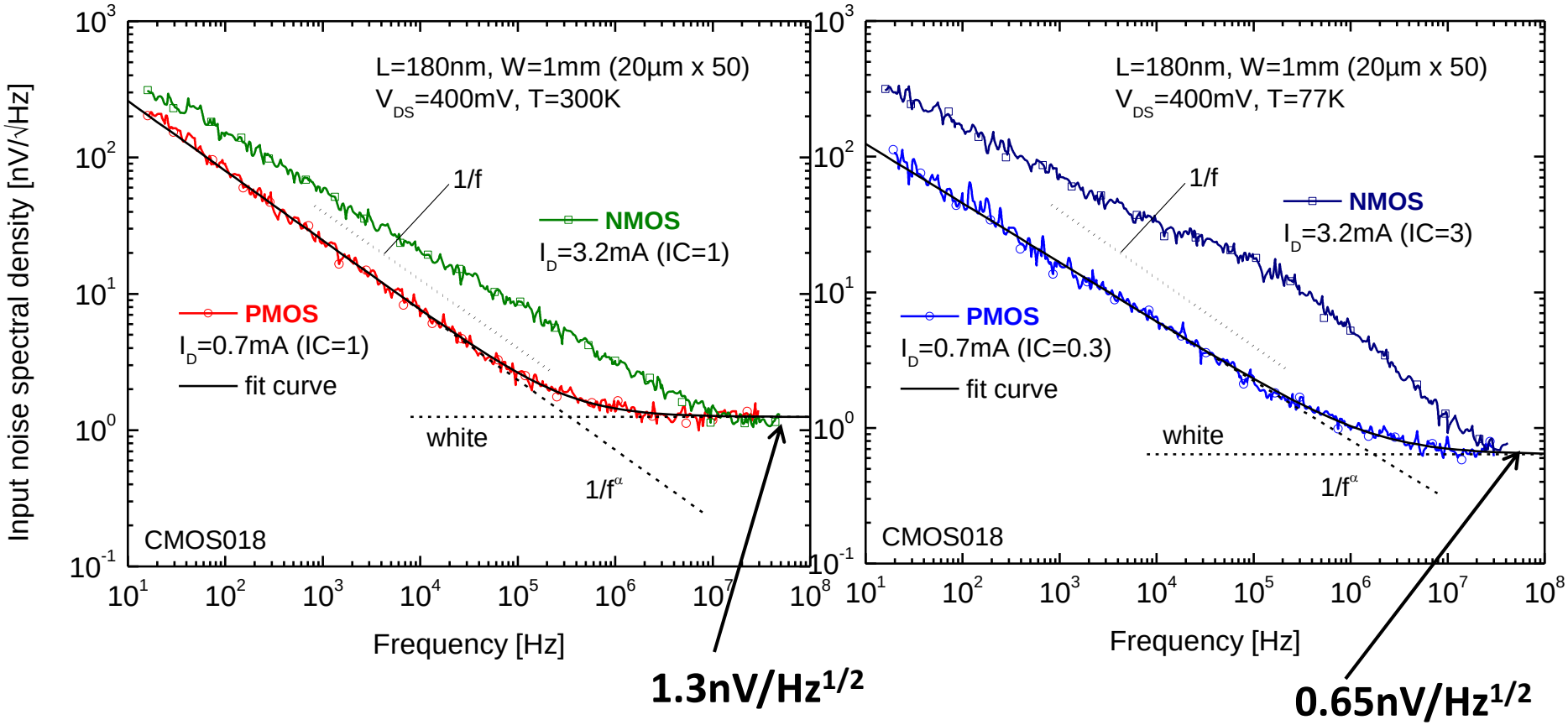


Transconductance/ /drain current ⇒

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \;\; at \;\; T = 300K \\ \sim 116 \;\; at \;\; T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases*, ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** ***g_m /I***, ***higher speed*** and ***lower noise***.

CMOS Noise Spectral Density *vs* T



TSMC 180nm: Noise lower by a factor of 2 at 77K across the spectrum for PMOS, only white for NMOS ; (1/f further reduced at longer L)

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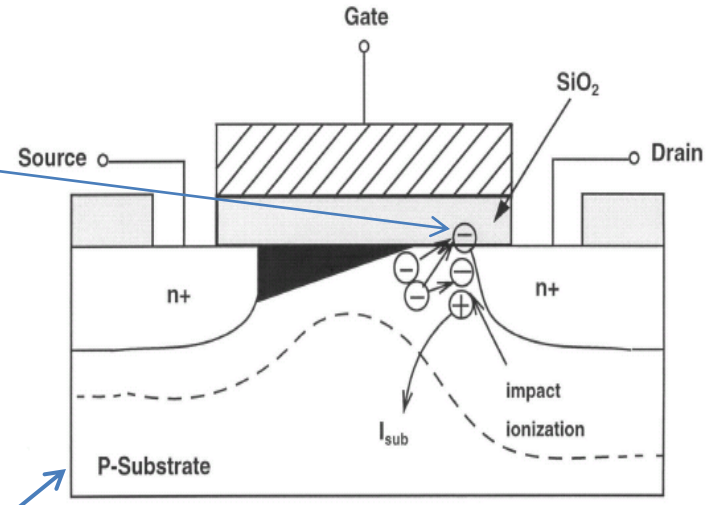
Impact Ionization and CMOS *Lifetime*

Chemistry slows down at 89K.

What is left of aging processes?

•***Impact ionization .*** Creation of *interface states* by (*some*) hot electrons causes a decrease in mobility, transconductance (gain), f_t , and a threshold shift.

• This limits the effective ***lifetime*** of the device at any temperature (defined in industry as *10% decrease in transconductance* g_m).



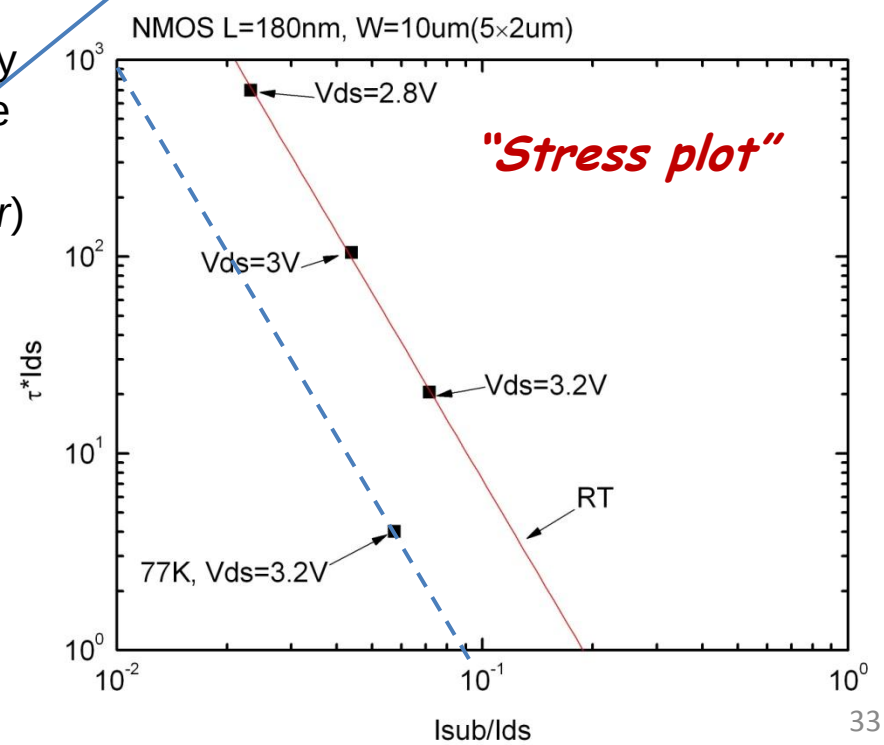
•***Accelerated lifetime testing*** is performed by stressing the device, at increased drain-source voltages and by measuring the ***substrate current*** (*a very sensitive quantitative indicator*)

.

$$\tau I_{ds} \Big/ W \propto \frac{1}{\left(I_{sub}/I_{ds}\right)^{a}}$$

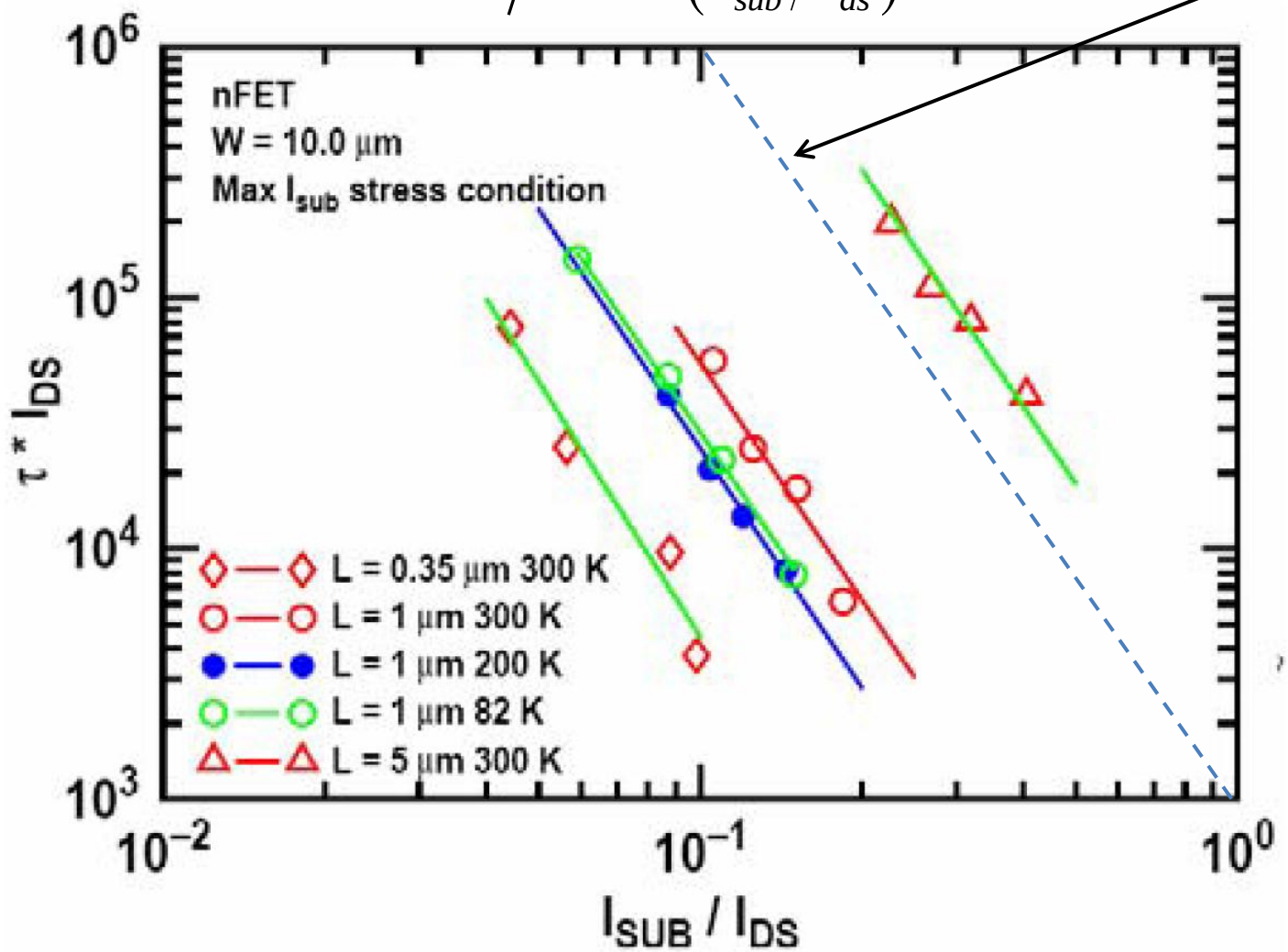
$$a = \varphi_{it} \Big/ \varphi_{i} \approx 2.9 - 3.2$$

$$\varphi_i \approx 1.3eV; \varphi_{it} \approx 3.7eV - 4.1eV$$

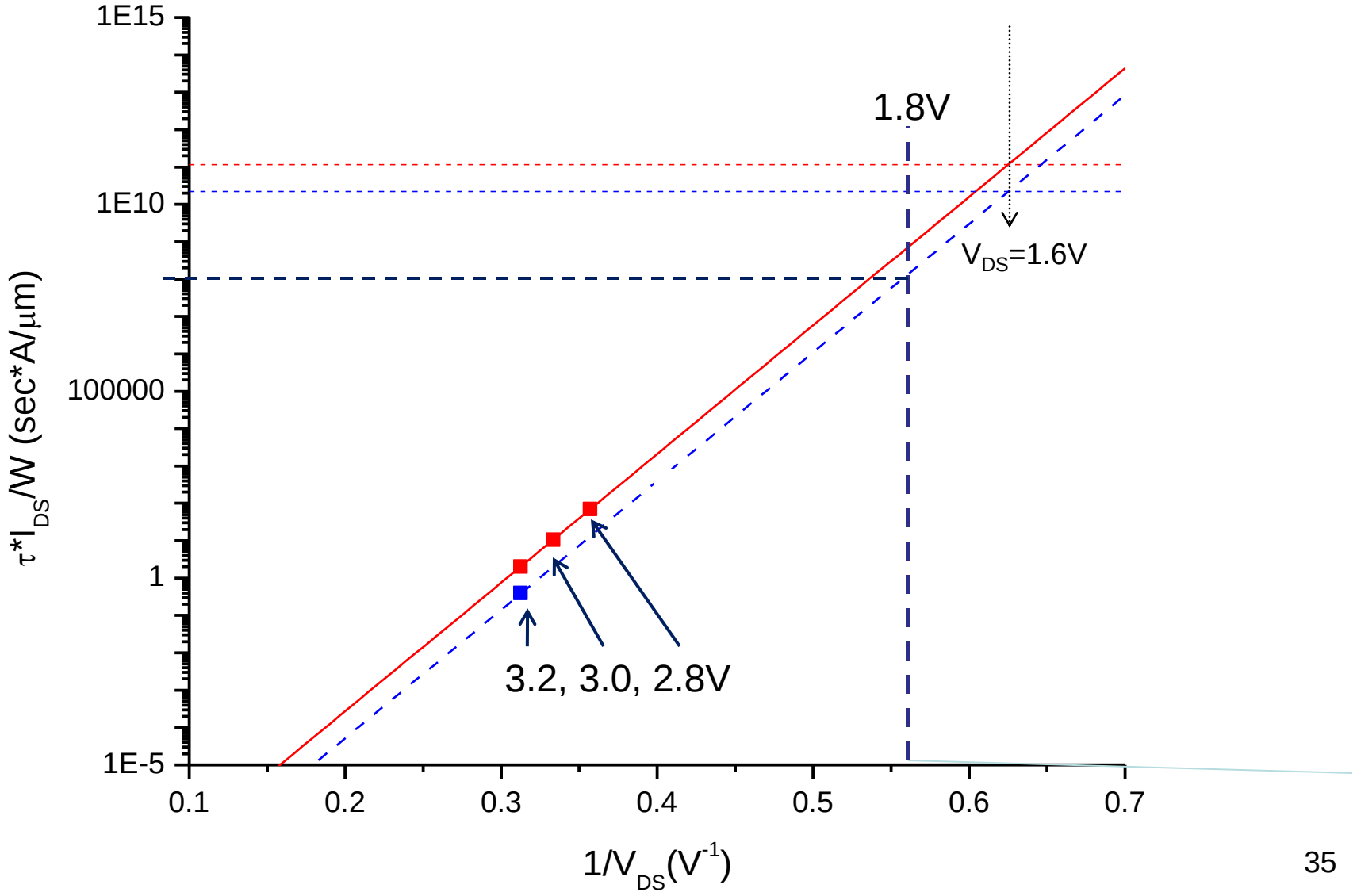


J. Cressler, et al. (Georgia Tech) measurements confirming:

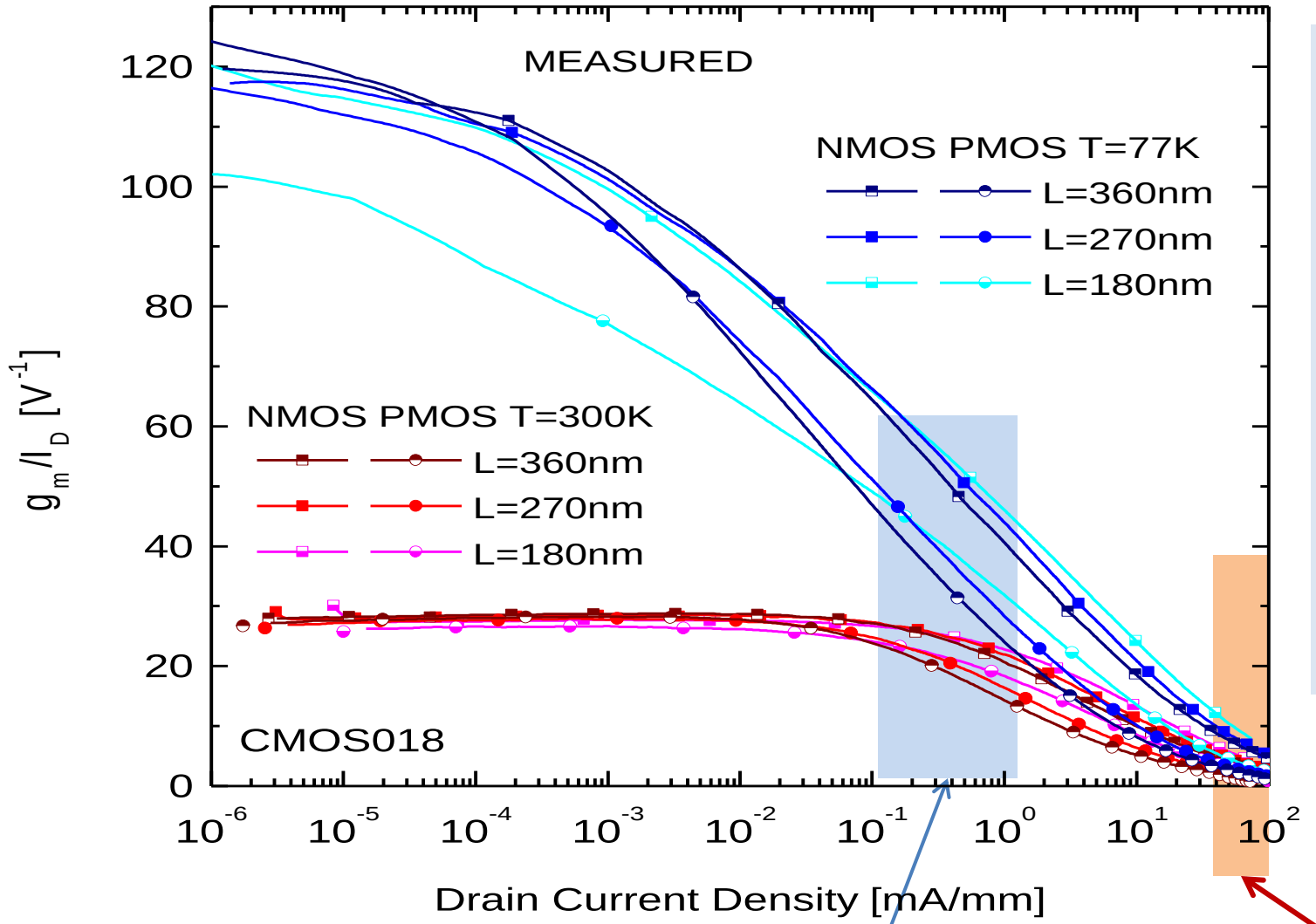
$$\tau I_{ds} \Big/ W \propto \frac{1}{\left(I_{sub}/I_{ds}\right)^{a}} \qquad a \square 3$$



NMOS 180nm TSMC lifetime vs Vds (preliminary)



Designing CMOS for low power = long lifetime



- *Lifetime* ≈ 1/(current density)
- Additional conservative guidelines: **V_{DD}-10%, L>1.5 L_{min}**

- *Digital*: **+** clock frequency **<<** ring oscillator frequency

Design region (approx.) for low power and long lifetime at 77K (moderate inversion)

Life time testing region

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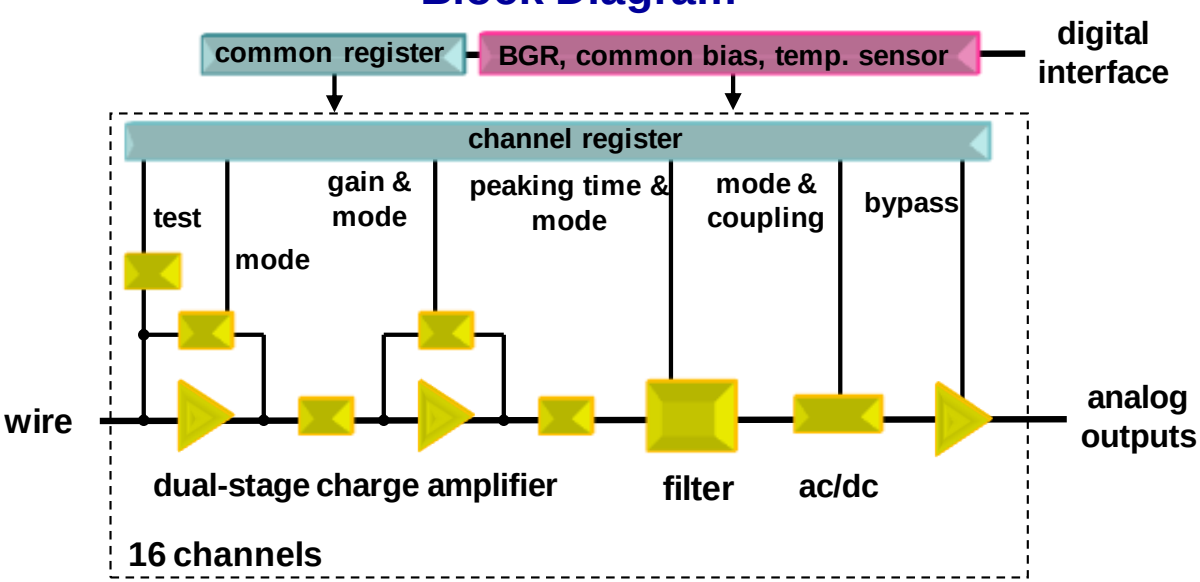
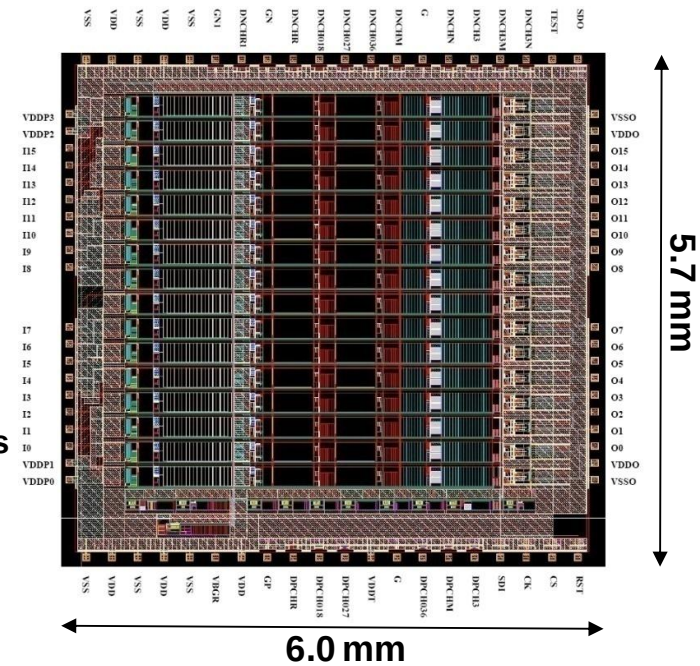
Analog ASIC

Block Diagram

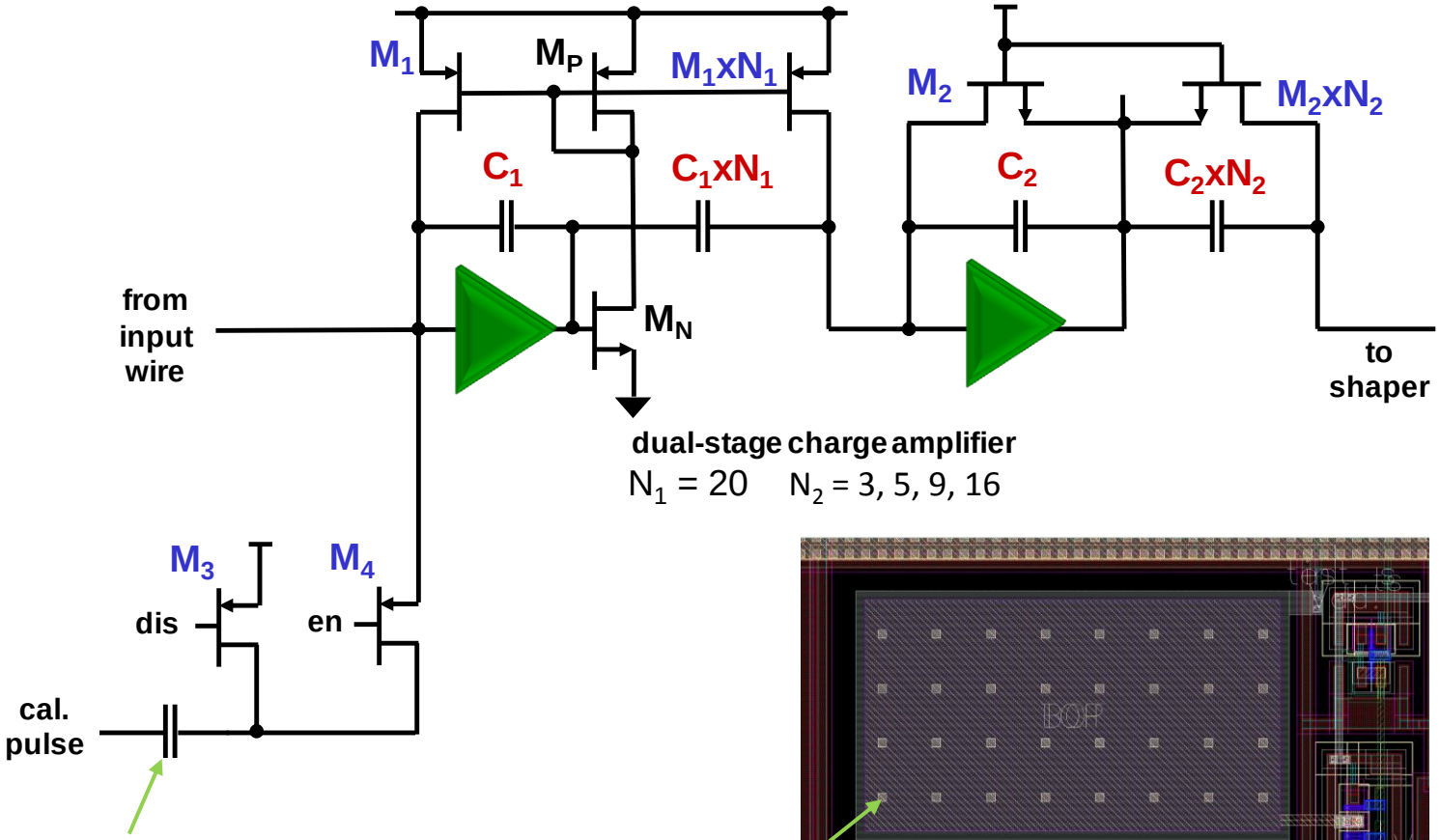




- 16 channels
- charge amplifier, high-order anti-aliasing filter
- programmable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
  programmable filter
  (peaking time 0.5, 1, 2, 3 μs)
- programmable collection/non-collection mode (baseline 200, 800 mV)
- programmable dc/ac coupling (100μs)

- band-gap referenced biasing
- temperature sensor (~ 3mV/°C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs
- **designed for room and cryogenic operation**
- technology CMOS 0.18 μm, 1.8 V

Cold Electronics ASIC - Front-End Detail and Calibration Scheme



$C_{INJ} \approx 180$ fF

Integrated injection capacitance (10 x 18 μm²)

Measured with high-precision external capacitance

$$C_{INJ} \approx \begin{cases} 184 \ fF \ at \ 300K \\ 183 \ fF \ at \ 77K \end{cases}$$

Integrated pulse generators on ASICs ➡ ***Charge sensitivity calibration of entire TPC during assembly, cooling and operation***

Outline:

1. Solar neutrino deficit and neutrino oscillations
2. Giant Lar facility plans (and dreams!)
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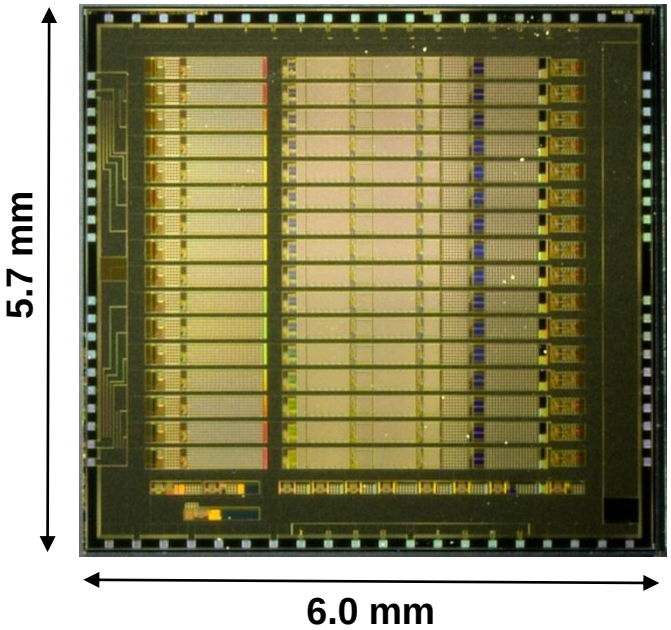
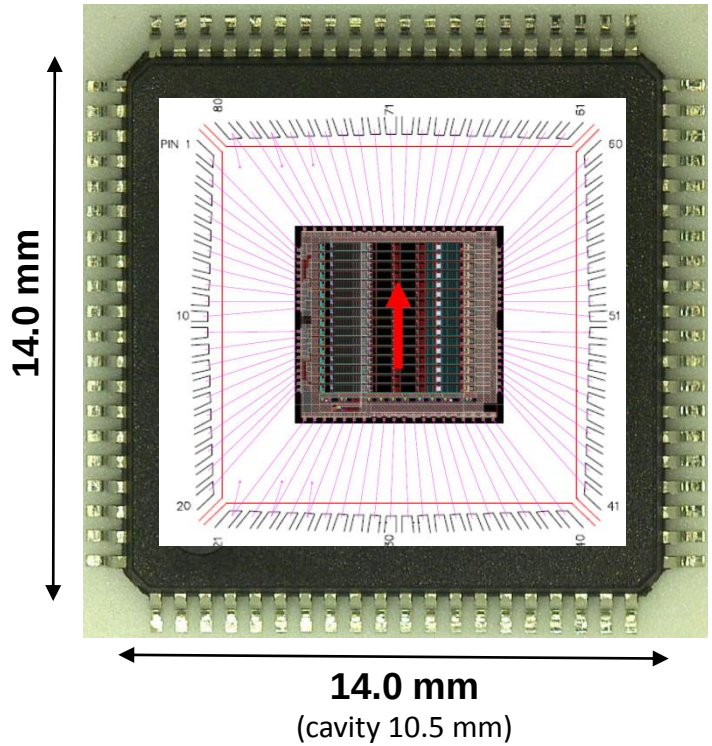
4. Giant TPCs readout challenge and essential block diagram
5. CMOS properties vs temperature
6. CMOS lifetime and electronics reliability
7. ASIC design
8. **ASIC results**
9. Summary and future developments

Analog ASIC: Die and Packaging, Temperature Cycling

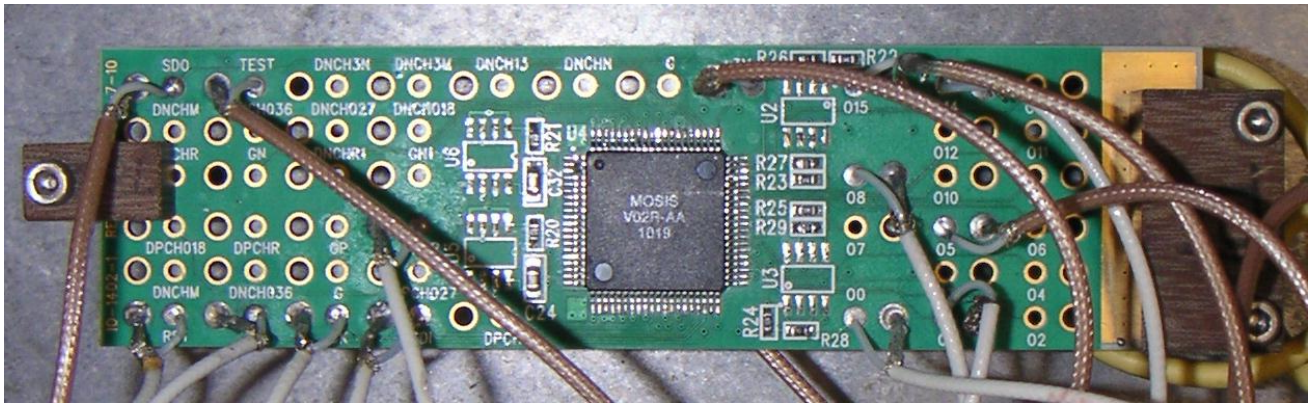
Die Photo



Package Photo



Test Fixture

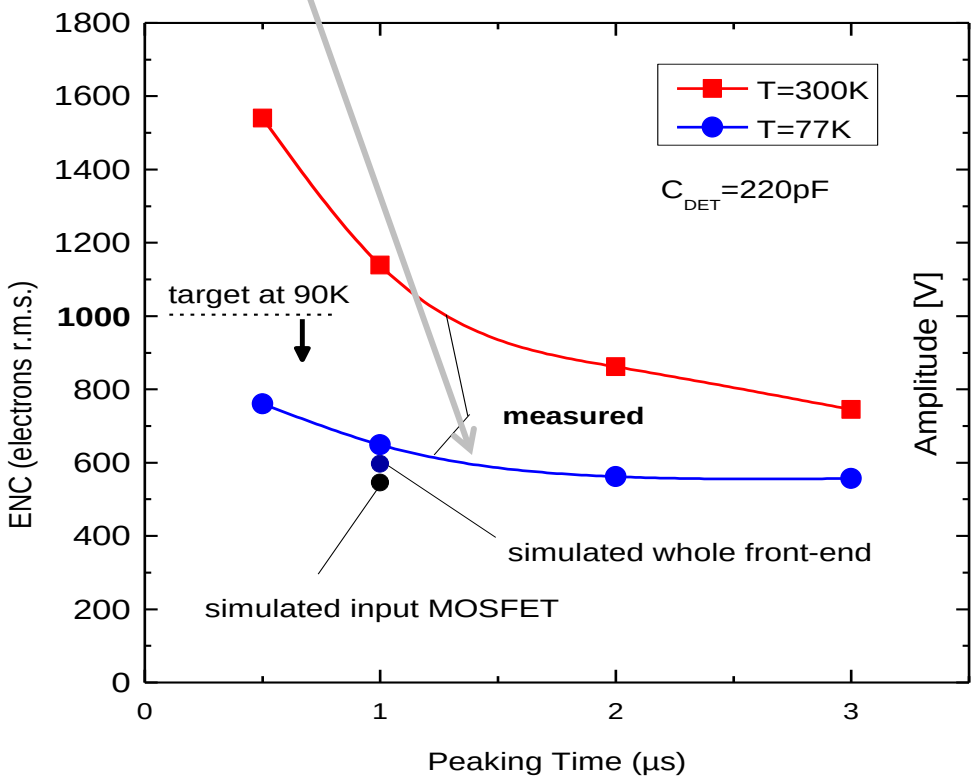


Cycled (abruptly, by pouring LN over the fixture in a dewar) from 300K to 77K more than 30 times

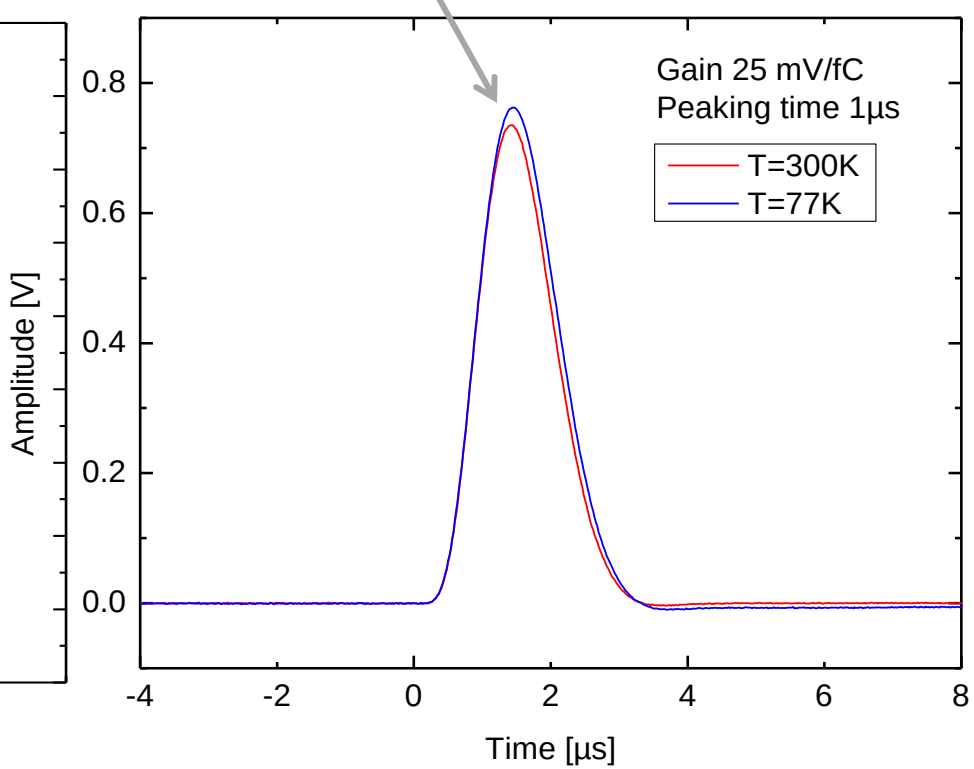
No failure occurred

Cold CMOS: Results from FE ASIC (1st prototype cycle)

Noise gets better at 77K (220pF det. Capacitance):



Signal after preamp+shaper changes little with temperature:



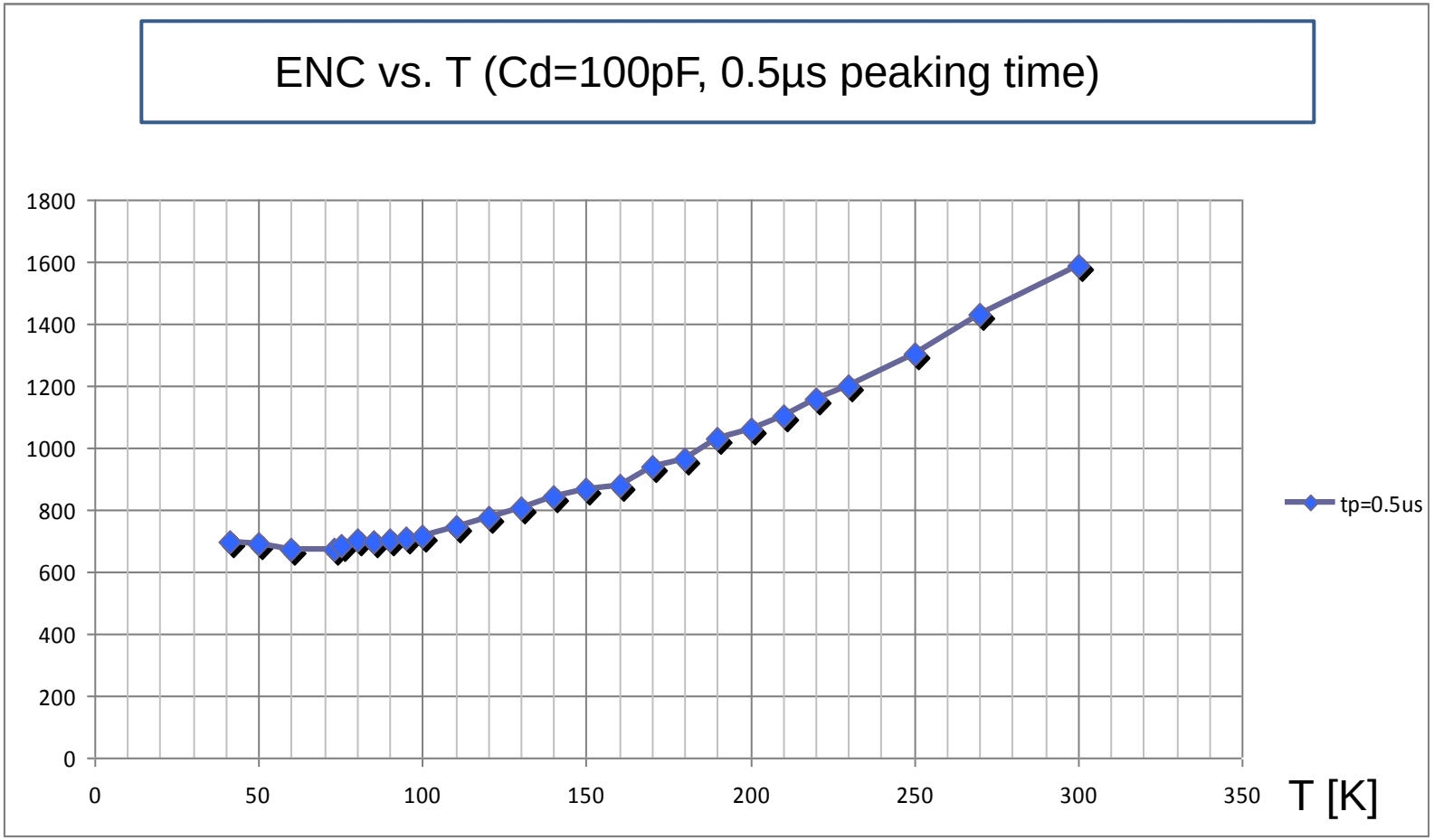
Integrated ***charge calibration*** capacitance
- <u>little change with temperature</u>

Measured with high-precision external capacitance

$$C_{INJ} \approx \begin{cases} 184\ \text{fF} & \text{at } 300\text{K} \\ 183\ \text{fF} & \text{at } 77\text{K} \end{cases}$$

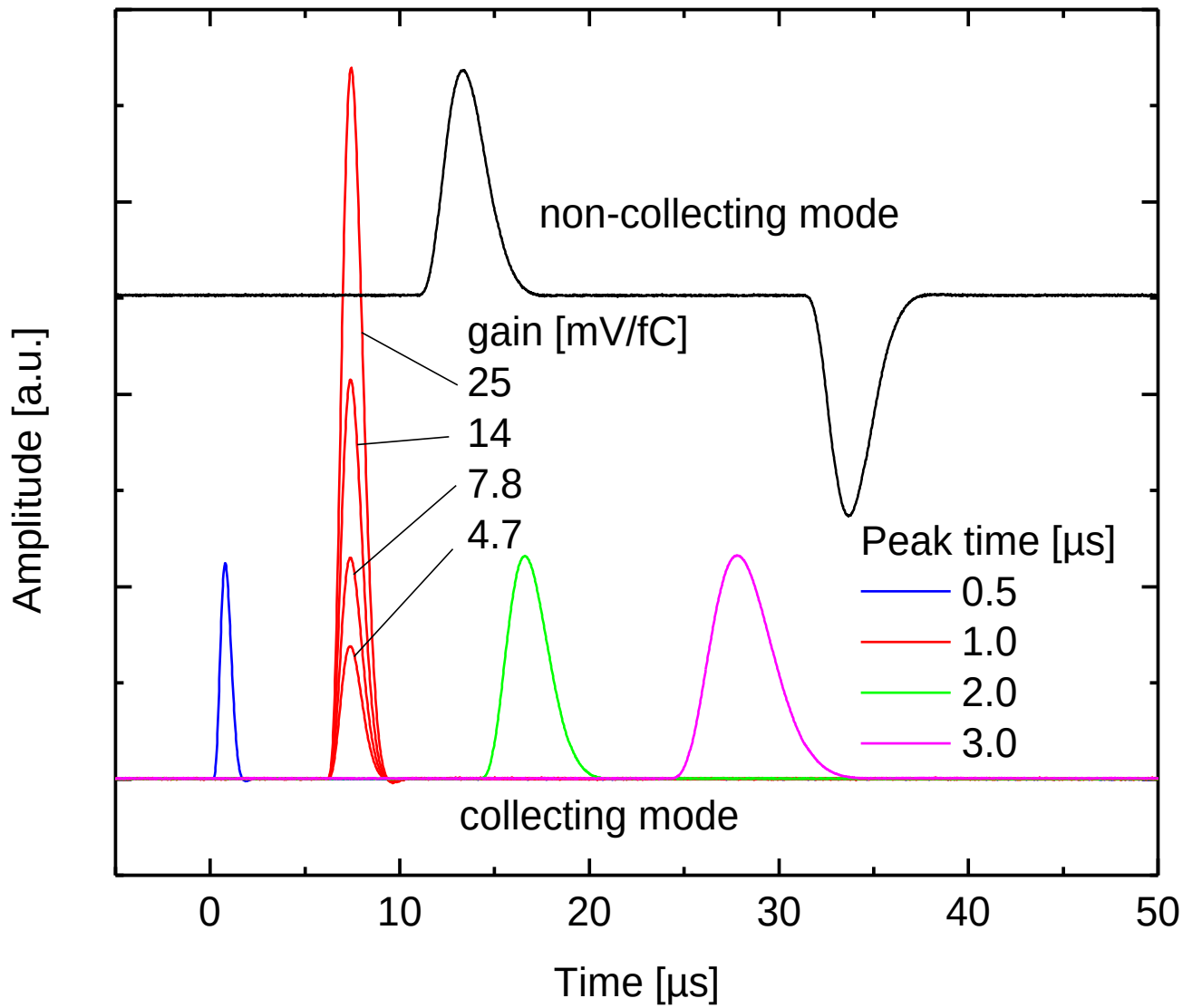
Noise *vs* T in CMOS:

Existing ASIC, 0.25 µm (not designed for Lar)



CMOS in LAr has less than half the (white) noise as that at room temperature, higher mobility and higher transconductance/current ratio

Signal Measurements: programmable gain, peak time and baseline



Bandgap Reference:

$$V_{BGR} \approx \begin{cases} 1.185\ \text{V} & \text{at } 300\ ^\circ\text{K} \\ 1.164\ \text{V} & \text{at } 77\ ^\circ\text{K} \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor:

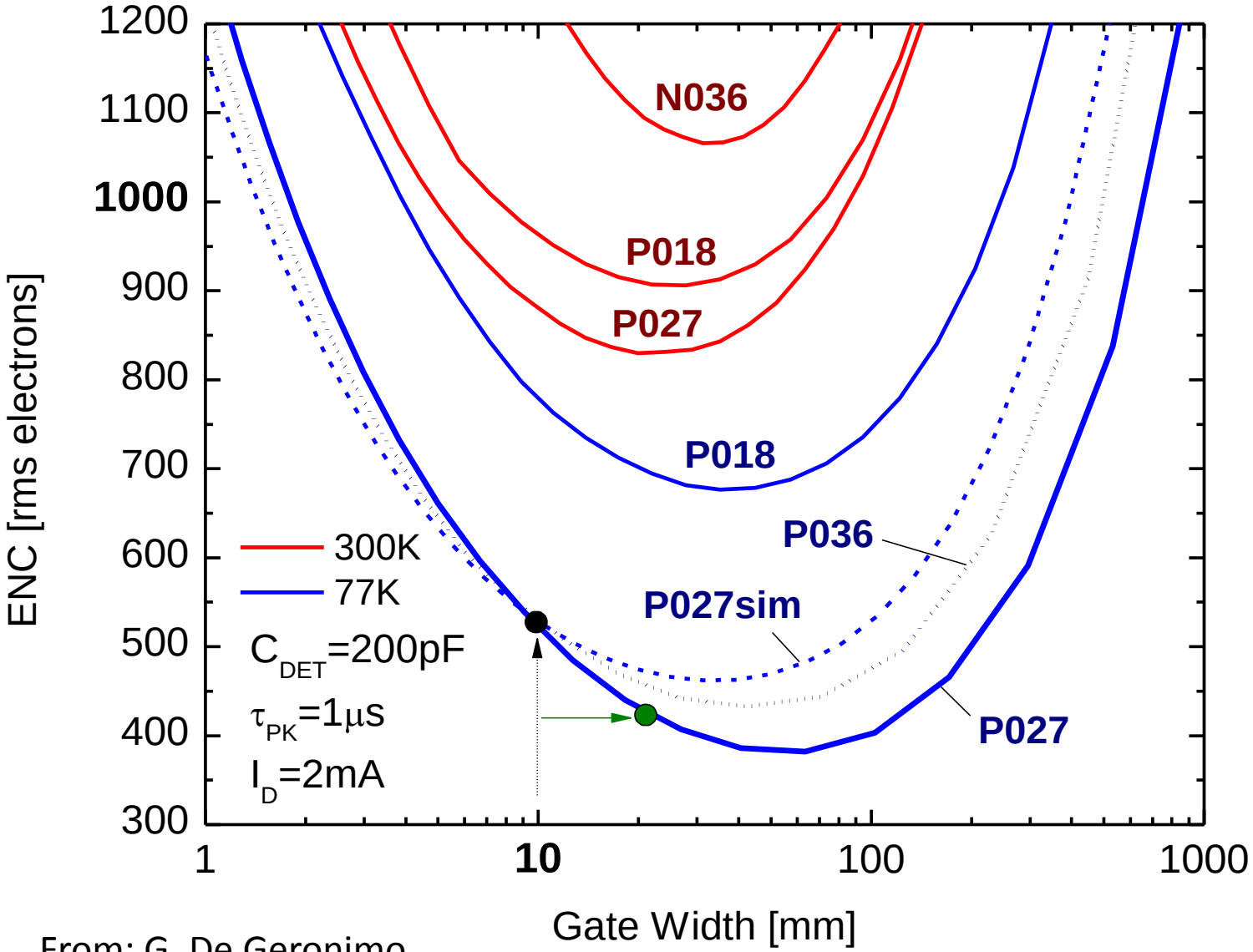
$$V_{TMP} \approx \begin{cases} 867.0\ \text{mV} & \text{at } 300\ ^\circ\text{K} \\ 259.3\ \text{mV} & \text{at } 77\ ^\circ\text{K} \end{cases}$$

~ 2.86 mV / °K

Programmable gain, peaking time and baseline

Maximum charge
55, 100, 180, 300
fC

Input transistor ENC optimization



From: G. De Geronimo

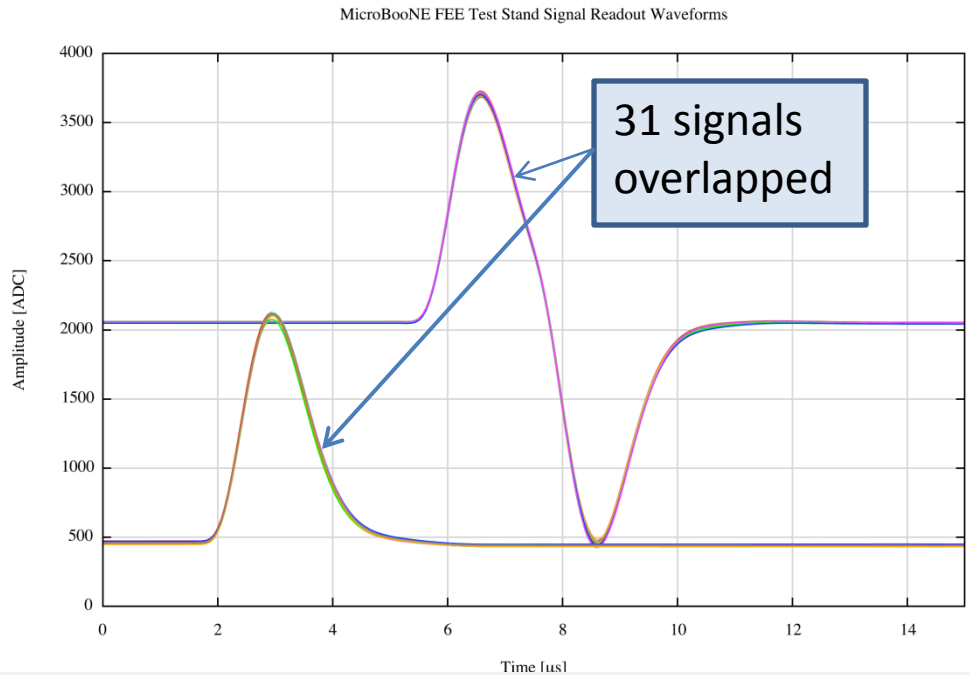
Analog ASIC: *gain and waveform uniformity*

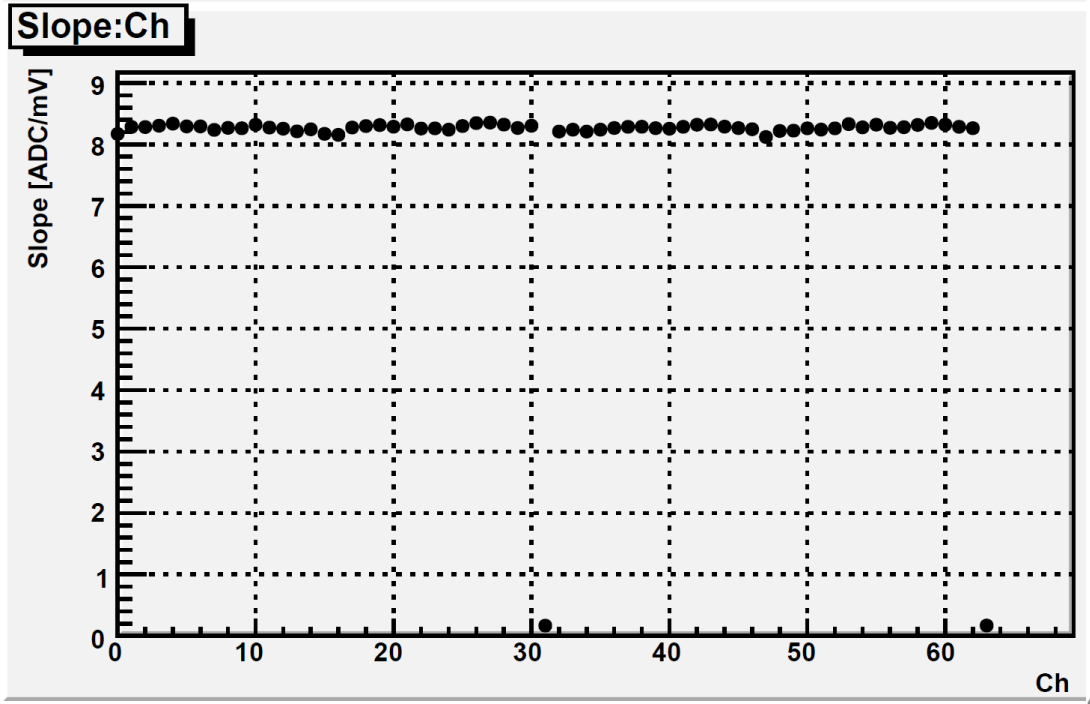
Four ASICs, **4x16** channels (one lead of the 32-channel cable not connected)

Residuals from a linear fit < 0.3%
Crosstalk < 0.3%

These measurements performed with enire MicroBooNE signal chain:
Analog ASIC+cold cable+ +intermediate amplifier+ADC

The ASIC will be used in *MicroBooNE* , ~150(75) ton LAr TPC





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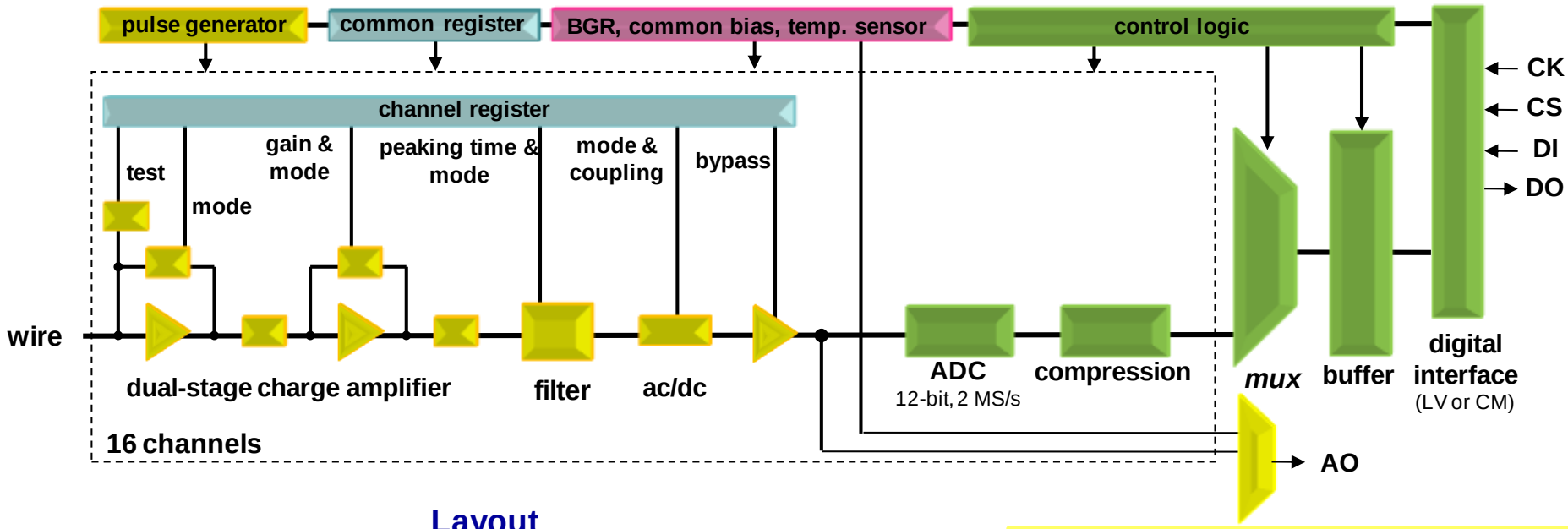
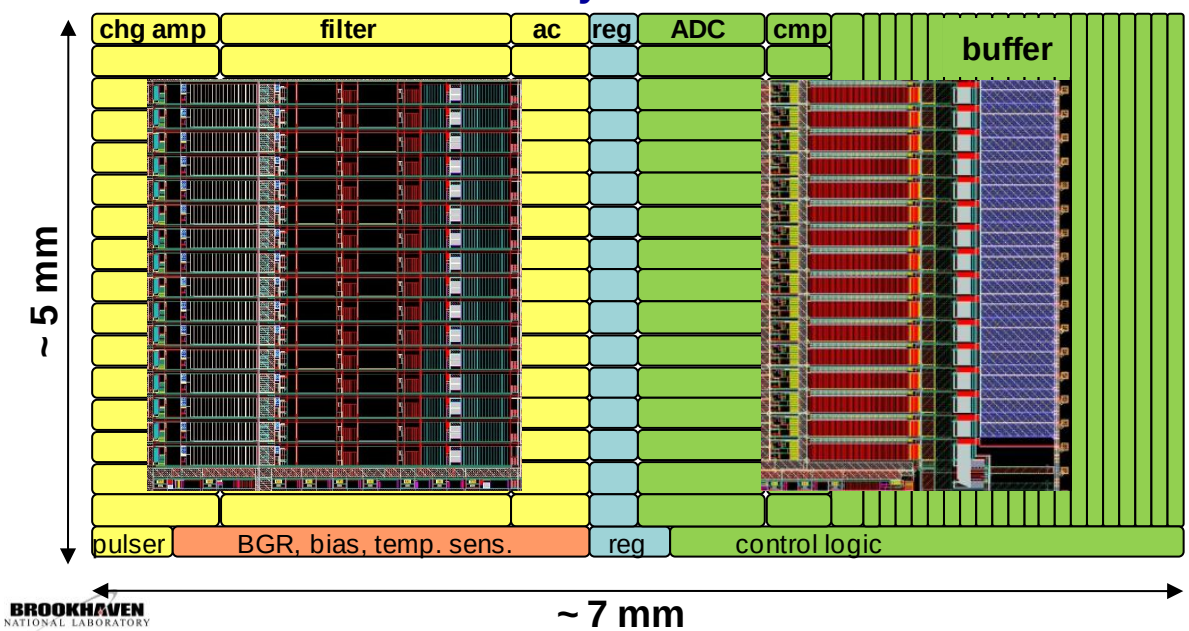
Front-End ASIC with 16:1 digital multiplexing

Block Diagram



Layout



- 16 channels
- charge amplifier (progr. gain)
- high-order filter (progr. time constant)
- ac/dc, progr. baseline
- test capacitor, channel mask
- ADC (12-bit, 2 MS/s)
- compression, progr. discrimination
- multiplexing and digital buffering
- LV or CM digital interface
- pulse generator, analog monitor
- temperature sensor
- estimated size ~ 6 x 8 mm²
- estimated power ~ 10 mW/channel

Summary and Future Work

- CMOS performs better at cryogenic temperatures
- CMOS technologies verified to work at 77K: IBM SiGe (Gergia Tech for Lunar Project), Chartered (FNAL) and TSMC (BNL); FPGAs (SMU, BNL); widest choice for a large project
- Defined and predictable design for 77-300K range
- Low-noise at cryogenic T demonstrated
  - ENC < 1,000 e^- at 200pF ~5mW/ch.
  - characterization and modeling of CMOS 180nm
- Low power design consistent with long lifetime
- <u>Future work</u>
  - Optimum technology node *wrt* dynamic range, noise, power
  - Merge separately developed ADC, zero-suppression & buffering

Backup slides

The primary science objectives of the LBNE Project are:

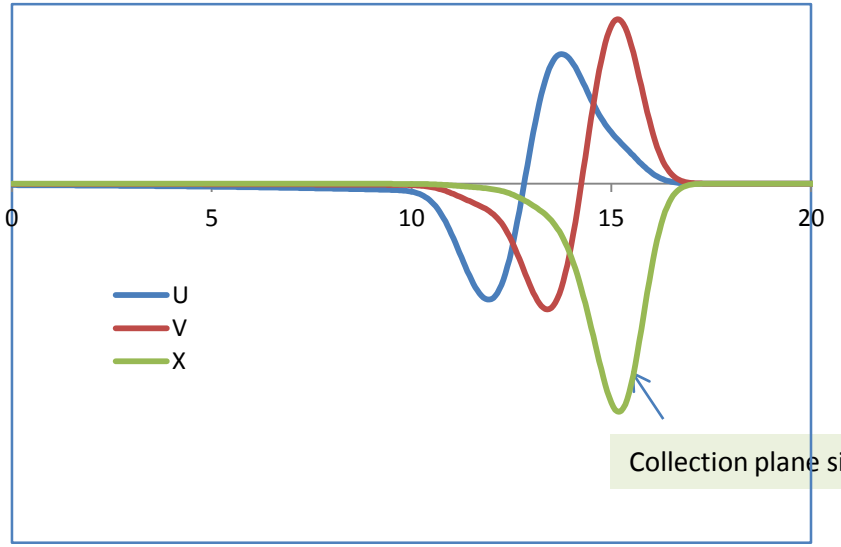
1. A search for, and precision measurements of, the parameters that govern $\nu_\mu \rightarrow \nu_e$ oscillations. This includes measurement of the third mixing angle θ_{13}, for whose value only an upper bound is currently known, and if θ_{13} is large enough, measurement of the CP-violating phase δ and determining of the mass ordering (sign of Δm^2_{32}).
2. Precision measurements of θ_{23} and $|\Delta m^2_{32}|$ in the ν_μ disappearance channel.
3. Search for proton decay, yielding a significant improvement in current limits on the partial lifetime of the proton (τ/BR) in one or more important candidate decay modes, e.g. $p \rightarrow e + \pi^0$ or $p \rightarrow K^+ \nu$.
4. Detection and measurement of the neutrino flux from a core collapse supernova within our galaxy, should one occur during the lifetime of LBNE.

Though outside of the primary objectives, the far detector placed at the proposed depth could enable studies of atmospheric ν physics, and with additional upgrades, studies of day/night ^{8}B solar ν physics and relic supernova neutrinos.

Track Waveforms on the Wires

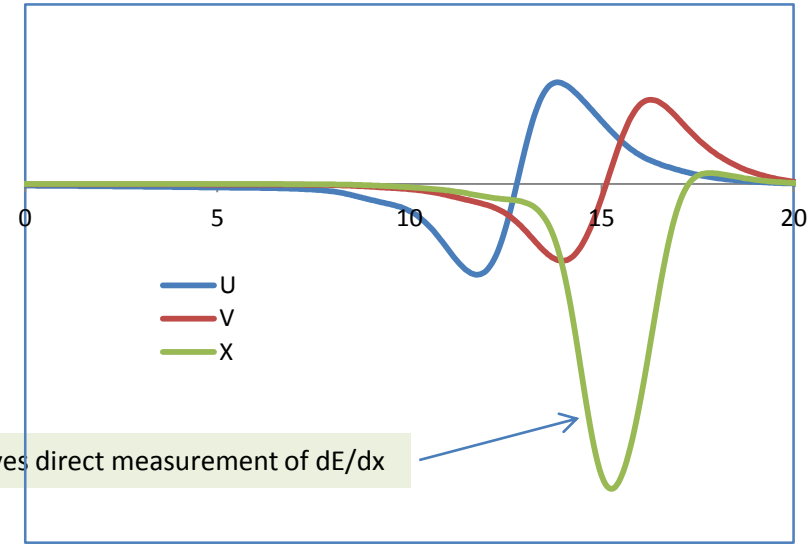
LBNE style wire arrangement: 3 instrumented wire plane + 1 grid plane
Raw current waveforms convolved with a 0.5μs gaussian (~1/2 drift length) to mimic diffusion

Current waveforms from a 0° track



Drift time [μs]

Current waveforms from a 45° track



Drift time [μs]

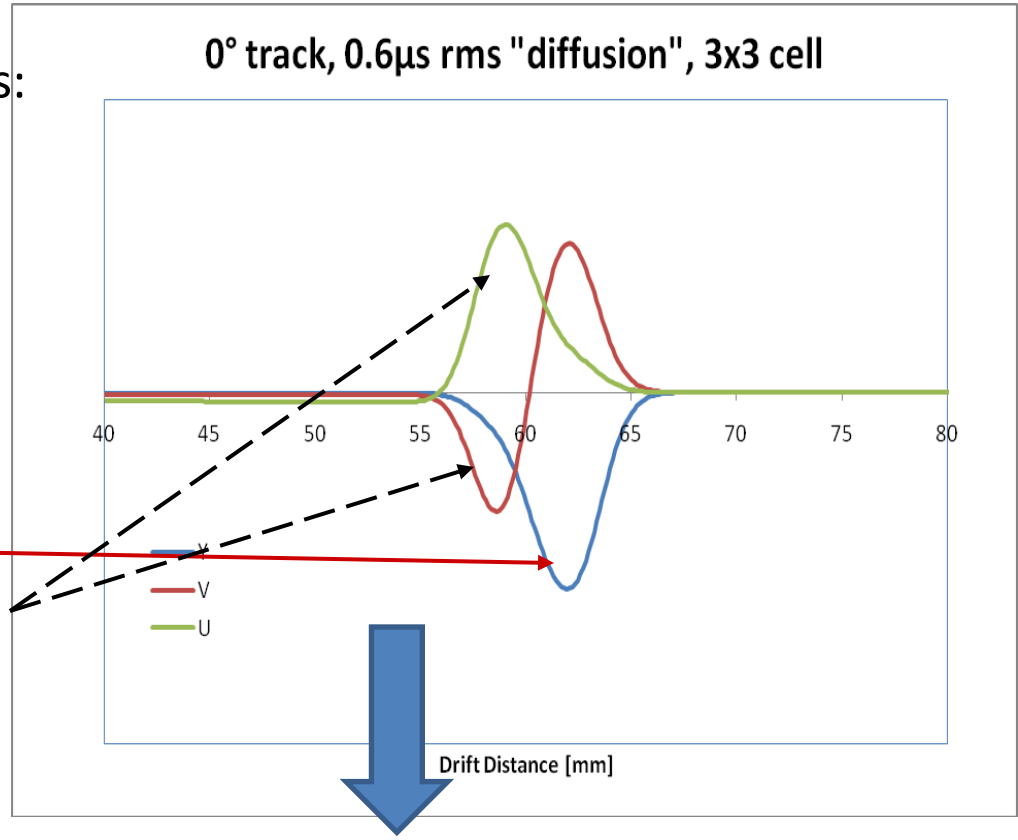
Collection plane signal gives direct measurement of dE/dx

Signals in LAr TPC

Charge signal:

- A 3mm MIP track should create *210keV/mm x 3mm /23.6eV/e = 4.3fC.*
- After a 1/3 initial recombination loss: *~2.8fC*
- Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368.
- The expected signal for *3mm* wire spacing is then ≈*1fC=6250 e*, … and for *5mm, ≈10^4 e*, for ***the "collection signal"***.
- The induction signals are smaller
- The ***time scale*** of TPC signals is determined by the ***wire plane spacing*** and ***electron drift velocity,*** *(~1.5 mm/μs at 500 V/cm).*

Induced Current Waveforms on 3 Sense Wire Planes:

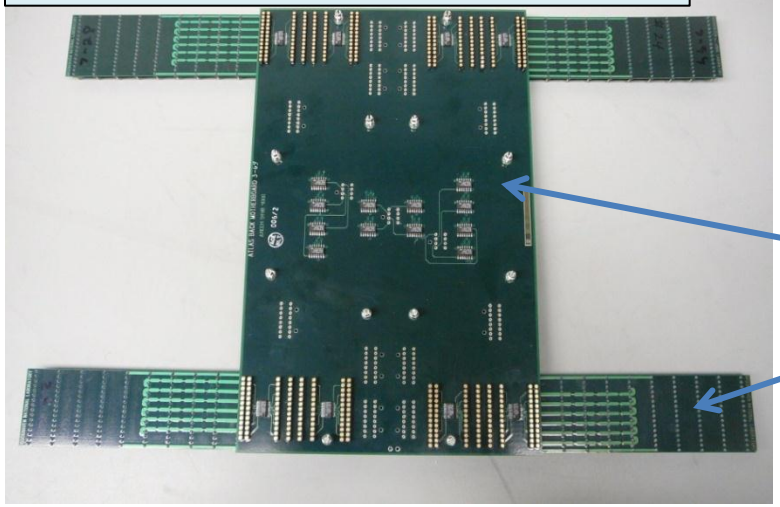


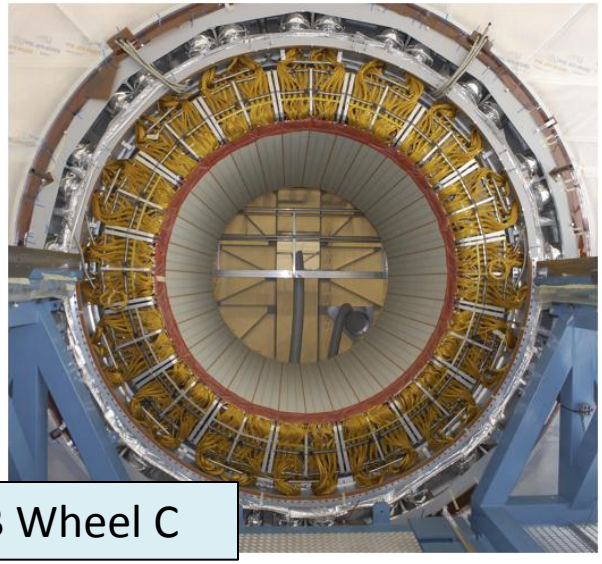
Sampling rate ***≤ 2 Ms/s***

Reliability of Cold Electronics (1) *wrt* *thermal contraction-expansion*

PCB and Cold Electronics in **ATLAS:**

EMB Mid/Back MB+SB Assembly





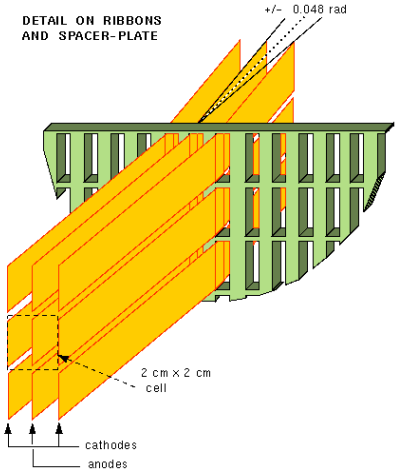
EMB Wheel C

- ATLAS LAr Calorimeter
  - **182,468** readout channels
- EM Barrel Mother Board and Summing Board
  - EMB has **~110,000** detector channels read out by 896x128-ch FEBs
  - **960** Mother Boards (MB)
  - **7,168** Summing Boards (SB)
  - **20,480** resistor network chips, **0.1%**
  - **~110,000** protection diodes on MBs/SBs
- EM Barrel Calorimeter has been cold since 2004
  - Operation: **7 years** so far
  - MB/SB will remain in operation without upgrade for super LHC

- **'Inoperative' channels <0.5%,** as of 05/10/2011
- **Dead channels in the cryostat ~0.02% since 2008**

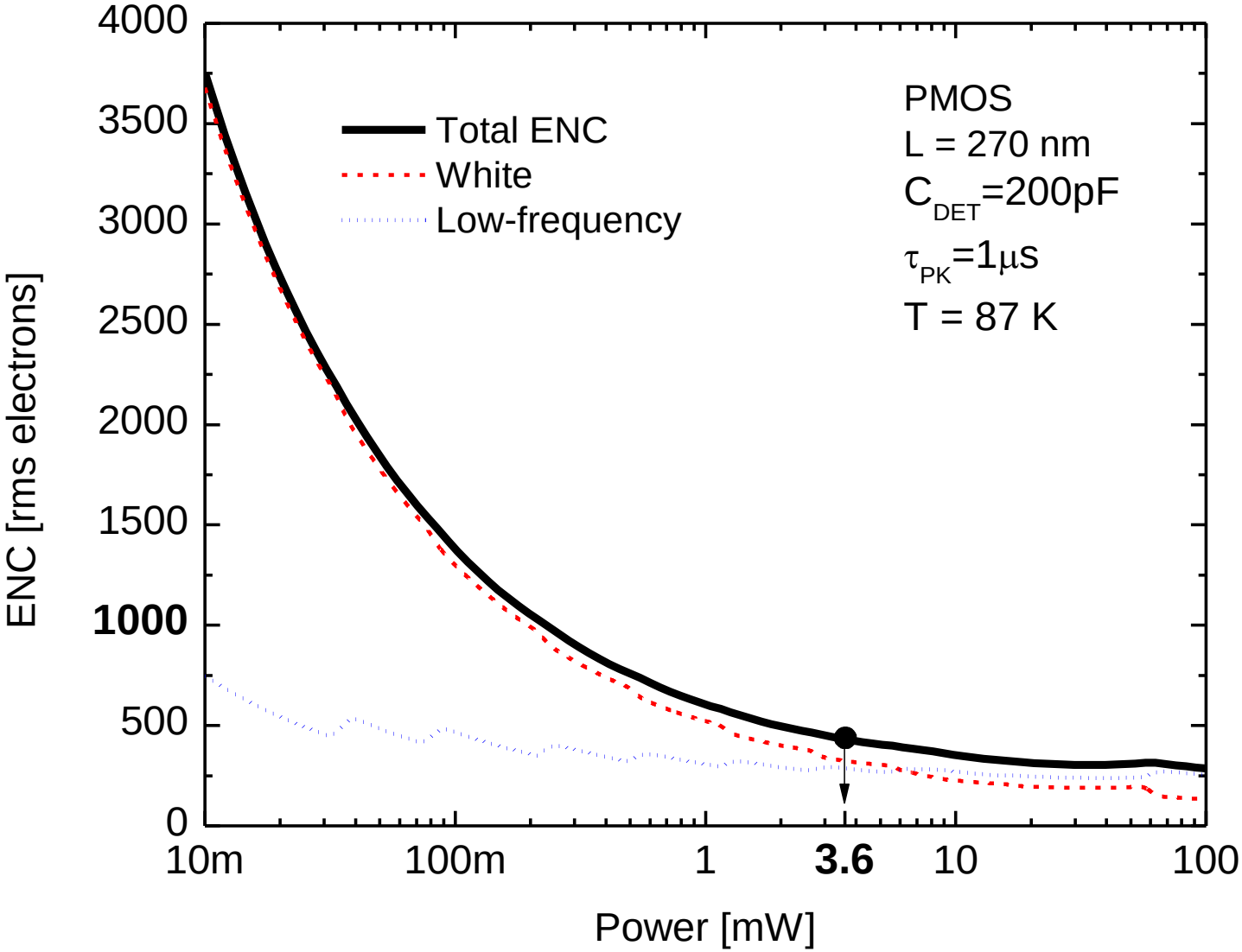
Reliability of Cold Electronics (2)

Cryogenic front-end based on JFETs –**NA48-NA62**



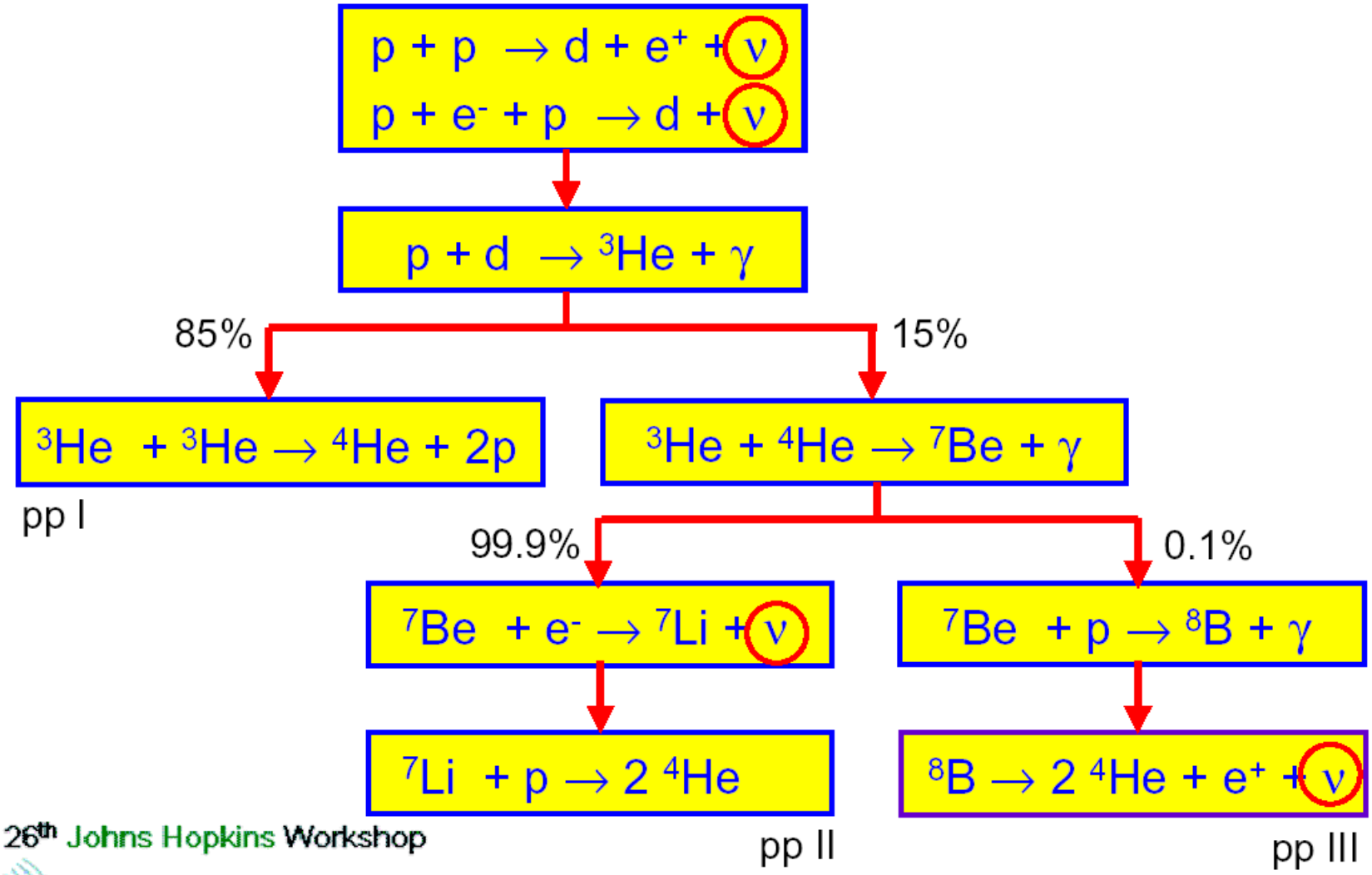
- Liquid Krypton calorimeter
- JFET preamplifiers in LKr: **13,212** channels
- Operated at very high voltage
  - Tested up to 7kV, operated in 3kV
- Failures
  - ~50 because of an HV accident in 1998
  - **~25** cold electronics failures after 1998, **< 0.2%**
  - The last failure recorded was more than 3 years ago
- Always kept at LKr temperature since 1998
- Operation
  - **13 years** so far
  - Plan to run until 2015, expected to be in operation for **17 years**

ENC vs power in the input cascode



Appendix 2

Solar hydrogen burning via the pp cycle



Supernova Neutrinos

- When a star's core collapses ~99% of the gravitational binding energy of the proto-neutron star goes into ν's

- SN at galactic core (10 kpc)
  $\Rightarrow$ tens of thousands of interactions in tens of seconds

- **Large detectors can discriminate between core collapse models**

Sanduleak -69° 202 → SN 1987A

"You don't have to be lucky, you just have to be patient."