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Development of a new Preamplifier-Shaper-Discriminator Chip for the ATLAS Muon Drift Tube Chambers in 130 nm IBM Technology

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We discuss the development and performance of a new analogue and digital readout chip for the Monitored Drift-Tube (MDT) chambers of the ATLAS muon spectrometer using the IBM 130 nm CMOS 8RF-DM technology. The 4-channel Amplifier-Shaper-Discriminator (ASD) chip was designed to match the analogue performance of the presently used device in 0.5 micron Agilent technology which is now obsolete. The new chip development is needed for the replacement of the front-end electronics of the existing MDT chambers by a more radiation hard version as well as for new muon drift-tube chambers with higher rate capability which are needed for high-luminosity upgrades of the Large Hadron Collider (LHC). Very good agreement was found between the simulated and the measured chip performance parameters, in particular the pulse shape, crosstalk, gain uniformity and noise. Results from a first neutron irradiation test will also be discussed.

Summary 500 words

The upgrade plans for the Large Hadron Collider (LHC) at CERN foresee an increase of the peak luminosity by a factor of up to 5 beyond the nominal value of 10^34 cm-2 s-1. The corresponding hit rates in the Monitored Drift Tube (MDT) chambers of the ATLAS muon spectrometer, mainly due to converted gammas and neutrons produced in the particle interactions in the detector, will lead to data rates in excess of the presently available readout bandwidth and to higher radiation damage, calling for at least partial replacement of the MDT readout electronics. For the front-end Amplifier-Shaper-Discriminator chip (ASD) we selected the IBM 130 nm CMOS 8RF-DM technology because of its accessibility via CERN and also in view of possible synergy with the front-end chip development for other ATLAS and LHC detector upgrade projects.

Each channel of the ASD chip contains a preamplifier, a three-stage shaper and a discriminator with lvds-output. One of the channels has an analogue output to monitor the pulse shape before the discriminator stage. In addition, a Wilkinson ADC for each channel, a DAC for programmable on-chip threshold generation, on-chip test pulse circuitry and JTAG controls have been implemented. As the pulse height is proportional to the supply voltage, on-chip LDO voltage regulation is used.
The chip is mounted on a 2-layer PCB and connected to an input protective network of identical design to the present system. In the chip layout, the low-resistive E1 and L1 layers of the 8RF-DM architecture were used for optimum on-chip grounding and supply voltage distribution.

Test pulse measurements showed very good agreement with the performance of the existing ASD chip as well as with the simulation. Gain uniformity between the channels of each chip and between different chips is within 2 %, cross-talk below 1.5 %. Noise corresponds to 6000 electrons (RMS) at 10 pF external capacitance, typical for the MDT readout. All measurements were done at the nominal supply voltage of 3.3 V, resulting in a power consumption of 24 mW per channel.

A first neutron irradiation test showed very little degradation of the ASD performance parameters as expected.

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