MICROROC: MICRO-Mesh Gaseous Structure Read-Out Chip

C. Adloff[1], J. Blaha[1], M. Chefdeville[1], A. Dalmaz[1], C. Drancourt[1], F. Dulucq[2], A. Espargilière[1], R. Gaglione[1], N. Geffroy[1], J. Jacquemier[1], G. Martin-Chassard[2], J. Prast[1], N. Seguin-Moreau[2], Ch. de la Taille[2], G. Vouters[1]

[1]*Laboratoire d'Annecy le Vieux de Physique des Particules, Université de Savoie, CNRS/IN2P3, Annecy-le-Vieux, France*
[2]*Laboratoire de l'accélérateur Linéaire / Omega, Université Paris-Sud, CNRS/IN2P3, Orsay, France*

Introduction

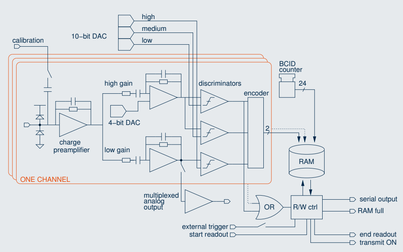
MICRO MEsh GAseous Structure (MICROMEGAS) and Gas Electron Multipliers (GEM) detectors are two candidates for the active part of a Digital Hadronic CALorimeter (DHCAL) as part of a high energy physics experiment at a Future Linear Collider (ILC/CLIC). Physics requirements lead to a highly granular hadronic calorimeter with up to thirty million channels with probably only hit information (digital calorimeter).
To validate the concept of digital hadronic calorimetry, a cubic meter technological prototype, made of 40 planes of one square meter each, is compulsory. Such a technological prototype involves about 400 000 electronic channels, thus requiring the development of front-end ASIC. Based on the experience of previous ASICs (DIRAC and HARDROC) and on multiple test beam results, a new ASIC, called MICROROC for MICRO-mesh gaseous structure Read-Out Chip, has been recently developed at IN2P3 jointly by OMEGA/LAL and LAPP microelectronics groups. It was submitted to foundry in June 2010, and prototypes were delivered at the beginning of September, a low volume production has been tested in 2011 and the detector testbeams have been performed in summer 2011 at CERN/SPS.

MICROROC Design

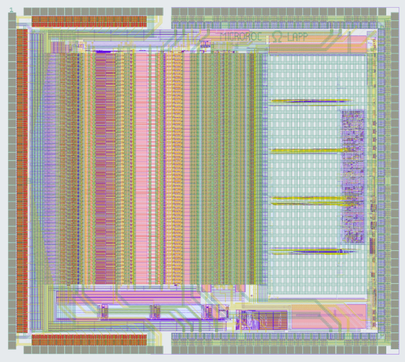
MICROROC is a 64 channels integrated circuit, made with AMS SiGe 0.35 µm technology. Each channel consists in:

- A sparks protection network;
- A charge preamplifier;
- Two shapers (low gain and high gain);
- Three discriminators with a 2-bit encoder;
- A 127 events digital memory.

MICROROC operation is tight by ILC beam structure requirements, and divided into two main phases. During the first phase the beam is on: for each channel, the detector signal is collected and the resulting charge is compared to three defined thresholds, every 200 ns the result is latched and stored inside digital memory if at least one channel has a charge above the lowest threshold (auto-trigger mode).
During the second phase, between two beam bunch trains, the analog part is powered down, and a serial daisy-chained readout is performed. For beam test operation, an external trigger is available, as well as an analog multiplexed readout for detector fine characterization.
A 4-bit DAC per channel is included to tune the reference voltage of the high gain shaper and thus compensate its offset, in order to reduce inter channels disparities.



MICROROC architecture

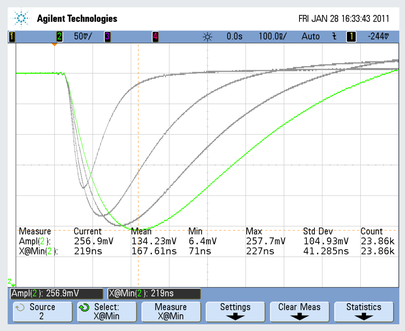


Layout

Prototypes Performances

The following characteristics have been established with the five prototype of the MPW run:

- Dynamic range: 500 fC and 200 fC for low and high gain path respectively;
- Preamplifier gain of 2.38 mV/fC;
- Noise rms: 1 fC at preamplifier output, 0.24 fC with 200 ns shaping (C_{det}: 80 pF for 1 cm^2 anode);
- Peaking times: 75, 115, 150 and 200 ns.
- 10-bit threshold DAC: linearity better than 3 DAC units;
- 4-bit pedestal adjustment DAC: linearity better than 1 DAC unit;
- Lowest threshold: about 0.7 fC.



Shaper test point output

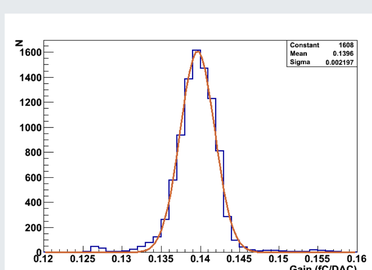
Production Tests

After prototype characterization, 341 chips have been produced, packaged in TQFP160 and individually tested. The production tests have consisted in:

- Testing digital interface with the chip and configuration registers;
- Testing input bonding thanks to external capacitors;
- Drawing S-curve without injection, then extracting offline pedestal for each channel;
- Drawing S-curve with 50 fC, then extracting offline inflexion point;
- Plotting the gain for each channel and checking the value (must be within nominal ±10%).

The summary of these tests is given below:

- 6 faulty chips (configuration errors);
- 11 with packaging problem (bad bonding);
- 12 with bad gain (at least one channel);
- 2 to be retested (test socket problems);
- 312 OK.

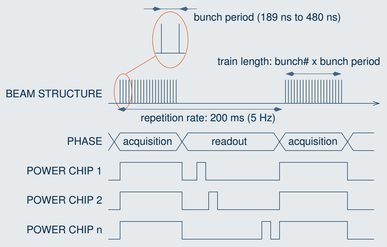


Gain dispersion for 144 chips

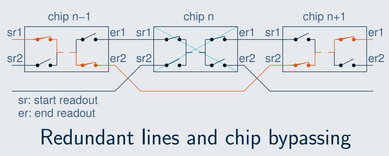
Yield: 91.5%. 288 of these chips are cabled on two square-meter MICROMEGAS detectors, and the 24 others are cabled to a spare ASU, used for laboratory tests, such EMC improvement or firmware development.

MICROROC Readout

Because of the very high number of electronic channels foreseen in the final detector, MICROROC will be embedded inside the detector and is designed to be daisy chained without any external circuitry, thanks to open collector output signals, to limit to a bare minimum the number of output lines on the detector.
There is one serial output which is transferred to the DAQ during the inter bunch. Moreover, during this inter bunch, the transceivers of chip which are not transmitting data are shut down to save power thanks to the POD (Power-On Digital) module.
The data format is: depth×(data×channels+BCID+chipID)



POD and readout timing



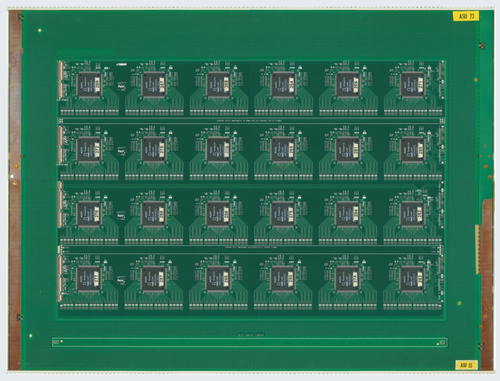
Redundant lines and chip bypassing

PCB and MICROMEGAS chamber design

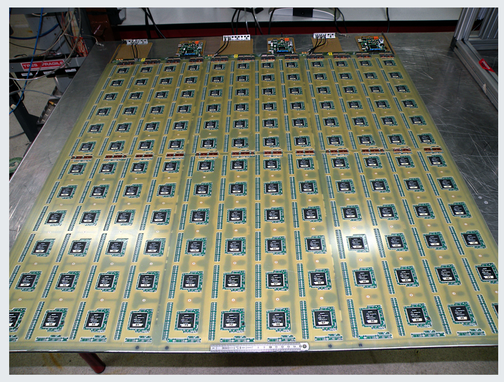
Each MICROMEGAS DHCAL square meter is divided into 6 PCB equipped with MICROROC on one side, and with the laminated mesh on the other side. These instrumented PCB are called ASU (Active Sensor Unit). Each ASU has 1536 readout channels (32×48 anodes). Pedestal and gain for every channel are carefully measured and verified at each of the following manufacturing process step:

- The 8-layer PCB cabling with ASIC, connectors and protection networks;
- The mesh lamination and the cut-out of the PCB to final dimension (32×48 cm^2);
- The baking of the mesh, up to 850 V in the air, to remove residual impurities between mesh and anodes.

Then, two ASU are connected together to form a SLAB, and three SLAB are laid and glued side-by-side to form a squared-meter detector.



(a) PCB with 24 ASICs



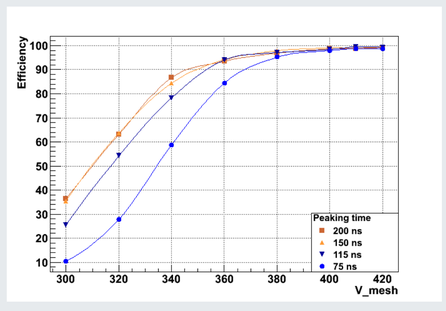
(b) Assembly of the detector

Preliminary Test beam Results

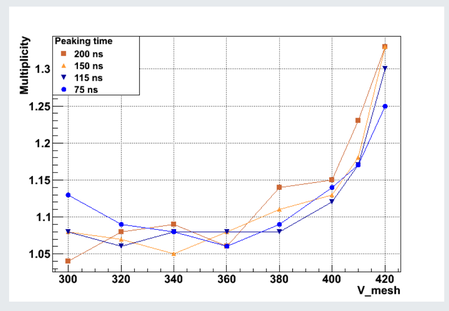
The 1st MICROMEGAS square meter prototype with MICROROC has been tested in muons and pions beams at CERN/SPS in august 2011 within the CALICE and RD51 collaborations. Two kinds of MICROMEGAS detectors (pad for coarse and strips for fine spatial resolution) acts as a telescope, and three scintillator paddles with PMT provided trigger signals. The following tests have been performed:

- Drift voltage scan (405 to 570 V);
- Mesh voltage scan (300 to 420 V) for different shaping times;
- Position scan (20 positions);
- Hadron showers;
- Different beam angle of incidence (0°, 30°and 60°);
- Trigger-less data acquisition: so-called RAMFULL mode (ILC operation).

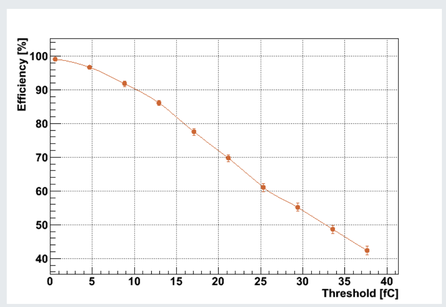
Preliminary results shows that the detector multiplicity is not correlated with the shaping time. Efficiency increase with shaping time, so that an optimum is found for each mesh voltage. The dependence of the efficiency as a function of the readout threshold plot is in very good agreement with those obtained in previous test beams with analog readout. Finally, the analog readout shows the expected landau distribution of the charge in the detector.



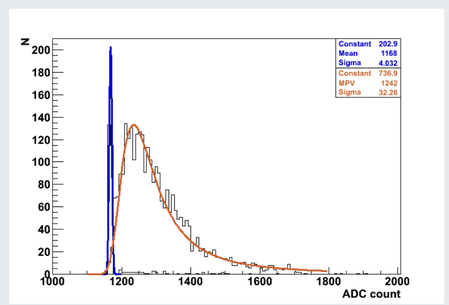
(c) Efficiency vs peaking time



(d) Multiplicity vs peaking time



(e) Efficiency vs threshold (Tp=200 ns)



(f) Analog readout

These results show that MICROMEGAS detectors are a good option for hadronic calorimetry near future linear colliders. The next steps are:

- Launch large production to equip a cubic meter calorimeter;
- Use full power pulsing capabilities in test beam;
- Rework DAQ to deal with large number of planes (on going);
- Enlarge detectors (aim: 1×3 m^2);
- Start R&D to suppress protection network on PCB (funded).

Presented by N. Seguin-Moreau at TWEPP 2011 conference