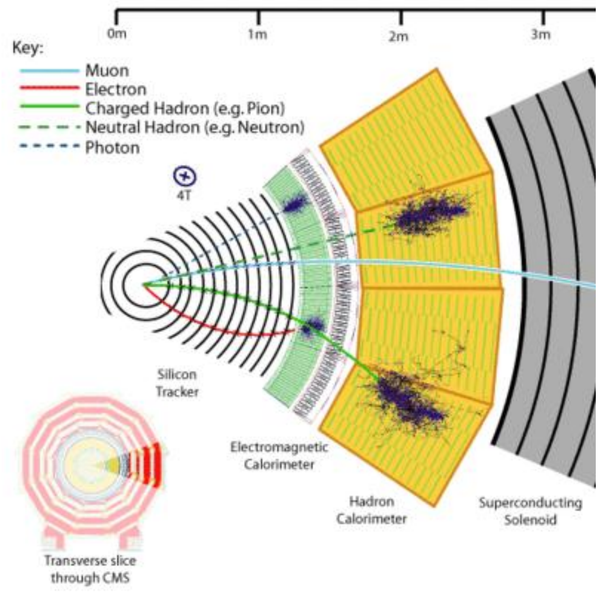
A front end chip for SLHC CMS strip tracker

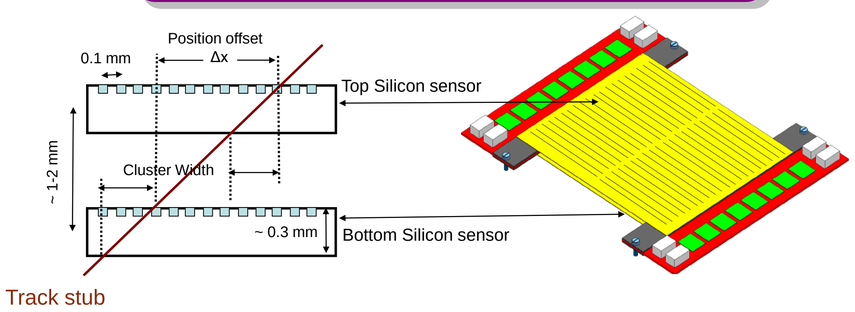
❖ Concept of Silicon strip Pt-module for CMS trigger purpose at SLHC

❖ CMS: One of the 4 major experiment of the LHC
❖ Run smoothly with 7Tev pp collision since 2010

❖ Upgrade :
- ❖ LHC luminosity to $5x10^{34}cm^{-2}s^{-1}$
- ❖ Preserve the performance by including the tracker in the level 1 trigger
- ❖ design chip for selective readout at the LHC clock (based on a local measurement of the particle bending)

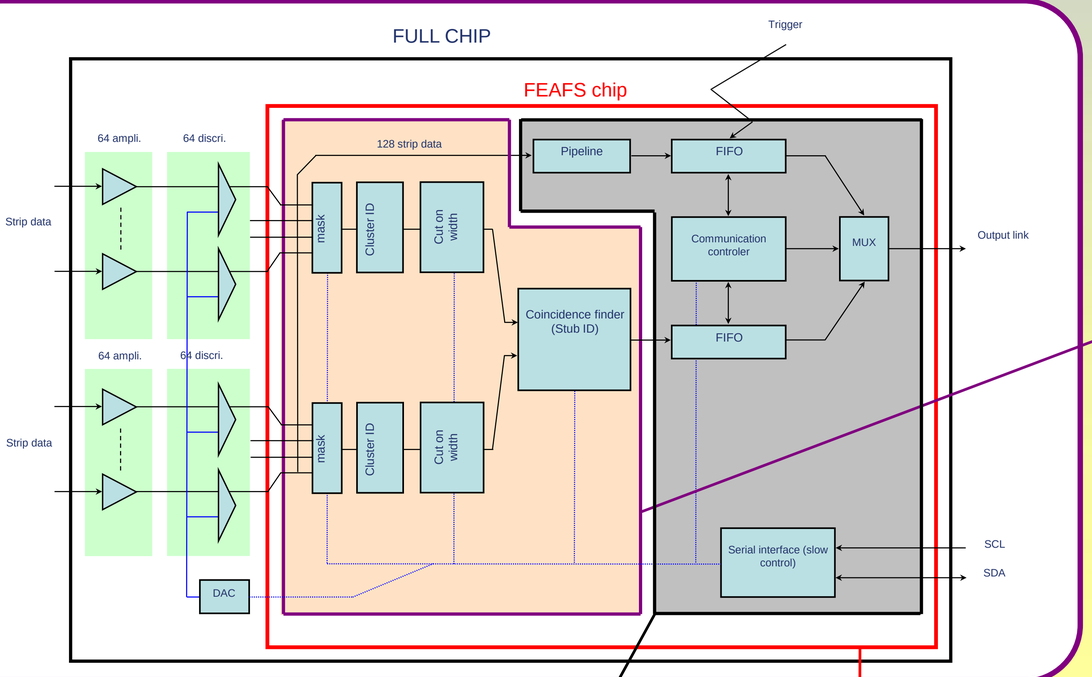


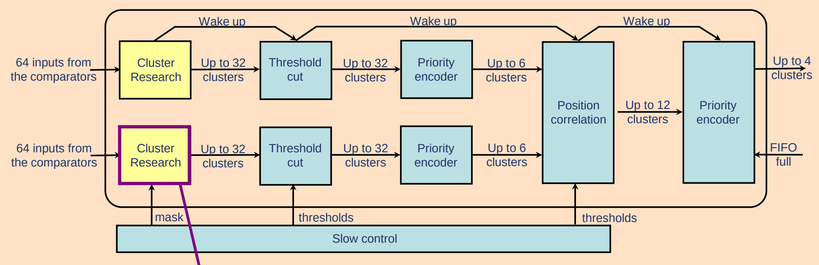
A Pt module for the sCMS silicon tracker



Track bending in the B-field is inversely proportional to transverse momentum
Cluster Width and Position Offset selection in 2 sensors connected to same Front End ASICs (Pt-module) allows to reject low Pt tracks, reducing band width for read-out of proper trigger information at the LHC clock frequency

❖ FEAFS chip : zero suppression and asynchronous architecture for selective readout



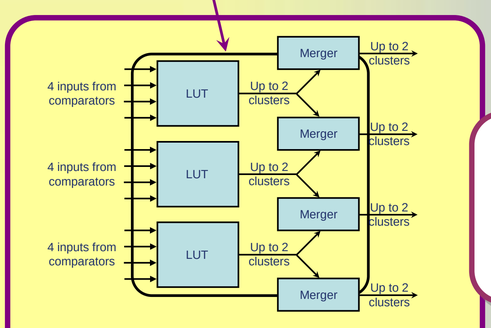


❖ clustering : identify and compute address of strips group

❖ cut on width : report clusters with a width below a threshold cut

❖ Position correlation : keep clusters if : $|Clust1+offset-clust2| \leq window$

❖ Threshold cut, offset and window : adjustable parameters by I2C.



❖ Algorithm based on a Look Up Table (LUT)

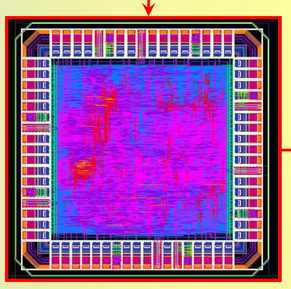
❖ 32 LUTs processes the 128 input strips within one clock cycle

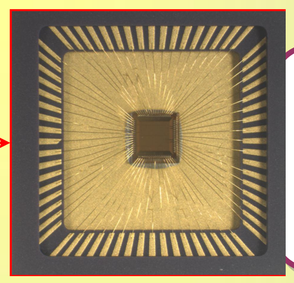
❖ Mergers re-assemble clusters eventually shared by several LUTs

❖ 2 FIFO of 16 words depth used to safely pass from LHC clock domain to the output link clock domain.

❖ A high throughput optimization on the output link :
- Readout and trigger data are merged on the same asynchronous output.
- Trigger data are zero suppressed.

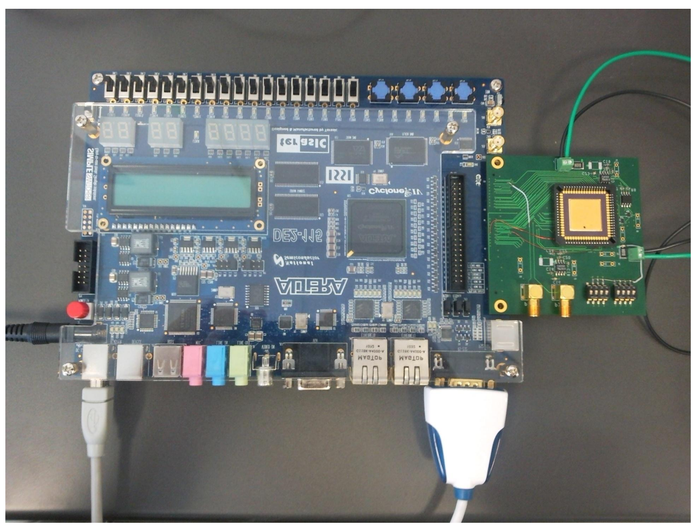
❖ Data latency depends on the strip occupancy .





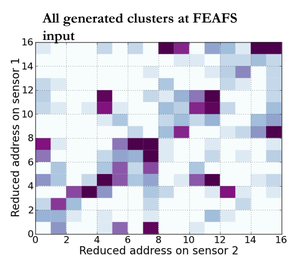
❖ First prototype developed in 130nm from IBM with approximately 60k VCAD Standard cells
❖ Only 32 inputs : internal demux to regenerate the 128 strips
❖ die Size: 4mm²
❖ Mounted in JLCC 68 pins

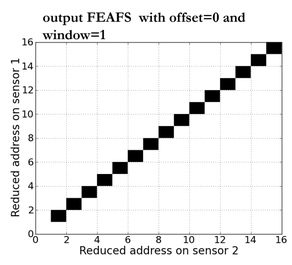
❖Test bench and results

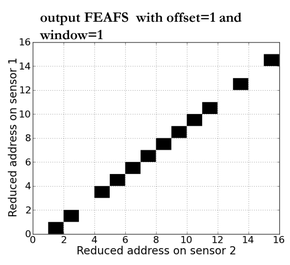


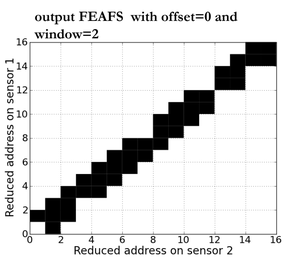
Test setup:
❖ ASIC test is done by a cyclone IV ALTERA FPGA (on a DE2-115 development board from TERASIC)
❖ test control is done either by USB, RS232 or JTAG.
❖ FPGA firmware : A random hit generation (with an adjustable probability) is applied on the FEAFS chip. The output bus is compared with an emulated FEAFS design in the FPGA.

Results:
❖ Power consumption at 40MHz : 75 mW (30 mW used in the 160MHz strip input PAD which will be removed when the analog part will be integrated)
❖ Internal logic is working as expected at 40 MHz frequency.









❖Summary and Perspectives

FEAFS prototype, was developed in 130 nm IBM technology. It include the main foreseen features for the digital part of the Strip Pt-modules read-out (Cluster ID and selection, Stub identification, pipeline, FIFO, multiplexer, serial line).
Test results of the chip are in perfect adequacy with simulations.
The FEAFS is the digital part of the front end ASIC, it has to be coupled with an analog part (preamplifier + comparator). A new FEAFS version is now proposed with the analog part, proper data format and adaptation to the GBT (GigaBit transceiver system from CERN). The power consumption need also to be minimized, a new version of pipeline, output interface and clustering algorithm are under development.
More simulation with realistic SLHC event are needed to adjust the design parameters in order to minimize cluster losses and trigger latency.

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