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A front-end chip development for the sLHC CMS Silicon Strip Tracker

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FEAFS chip has been designed for a future sCMS Silicon Strip Tracker. Its primary function is to provide a 40 MHz selective readout of particle hits useful to establish the 100kHz hardware trigger of the experiment. To achieve this goal, the chip identifies clusters of limited number of activated strips and correlated in position in two closely superimposed sensors connected to the same chip. These data are sent on a shared link with the full detector read-out of trigger-accepted events. FEAFS chip has been developed in IBM 0.13µm technology. This poster presents the design of the chip and test results.

Summary 500 words

A full front-end chip for CMS silicon strip sensors at sLHC will include an analogical part, pre-amplifier and comparators, followed by a digital one. The FEAFS chip is proposed for this second part, dedicated to the data reduction and transfer to an optical link system driving the signal to the control room electronic boards.
In its present version, the FEAFS chip is limited to 2 groups of 64 channels. For each of them the first stage of the chip identifies clusters of strips above threshold, with an architecture based on look-up table, it applies a programmable cut on the number of strips and encodes the address. In the second stage, the cluster addresses in the two groups are compared with an offset and selected within a given window, both parameters are programmable. Eventually, a maximum of 4 selected cluster information can be found within one clock cycle (25ns), these data are referred in the following as the trigger data
In a third part of the chip the digital outputs of all channels are buffered in a pipeline build around a shift register allowing the storage during the 6.4µs latency of the first level (L1) trigger. According to the 40MHz clock, the shift register length is 256. These data are refereed in the following as the raw data.
The fourth part of the chip is the data link handling the L1 trigger and the shared output between the trigger and raw data paths. As the throughput of the output bus depends on the strip activity and on the L1 trigger rate, FIFOs are implemented for both types of data with a fixed depth of 16 words. The ability to have two different asynchronous clock domains allows to adjust the output bus frequency in order to prevent overflows. Finally, all the slow control is handled by an I2C like bus. It allows to configure the chip operating modes as well as the various cluster selection parameters.
In conclusion: a chip has been designed for implementation of data reduction for triggering purpose with the CMS Silicon Strip Tracker at SLHC. Although the specifications are not final, a first evaluation version has been submitted for foundry in the 0.13µm IBM process using the CERN VCAD standard cell. It has been designed using the Cadence tools. The layout size is about 2mm2, it uses almost 60k standard cell, most of them in the readout data pipeline that has currently been limited to a 135 register size. The chip was delivered in March of this year, the firsts testing results will be shown on the poster.

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