Contribution ID: **5** Type: **Poster**

The NA62 Liquid Krypton Calorimeter Readout Module

Thursday 29 September 2011 16:00 (2h 30m)

The NA62 experiment will be focused on precision tests of the Standard Model via studies of ultra-rare decays of the charged kaons. The high resolution Liquid Krypton (LKr) calorimeter of the NA48 experiment will provide a photon-veto with hermetic coverage from zero out to large angles from the decay region. The study of an upgraded readout system began in 2008.
This paper presents the Calorimeter REAdout Module (CREAM), an upgrade project for the backend part of the LKr data acquisition chain. The CREAMs will provide 40 MHz sampling of 13248 calorimeter channels, data buffering during the SPS spill, zero suppression, and programmable trigger sums for the experiment trigger processor.

Summary 500 words

The CREAM is a 1-slot wide VME 6U form-factor module. One module houses 2×16 channels 40 MS/s ADC with a 14-bit dynamic range and an ENOB greater than or equal to 10-bit. The external reference sampling clock will be provided by the Timing, Trigger and Control (TTC) system designed for the LHC experiments.
Each of the CREAM input channels consists of an AC-coupled differential line receiver and a pulse shaper. A 14-bit DAC allows tuning the DC offset of each channel in order to correctly adjust the pedestals and to preserve the dynamic range. The signal is shaped before the ADC input into a differential semi-Gaussian signal with a 40 ns rise time and a 70 ns full width at half middle (FWHM).
During the data acquisition, the CREAM inputs are continuously digitized and written into an on-board pipeline memory. When the L0 trigger occurs, the control logic freezes the corresponding data samples from all channels or copies them in another memory partition for subsequent L1 trigger decision or readout.
The L0 trigger latency should not exceed 10 ms and the module must be able to store locally up to 400×10ˆ3 14-bit samples per channel. The size of the data buffer is defined by the L0 trigger rate (1 MHz), the number of samples per event and by the duration of the data-taking phase (accelerator burst time, typically up to 10 s with a period of up to 50 s). For that reason, 4 GB DDR3 SODIMM is chosen to ensure necessary storage capacity for data from 16 channels (2.56 GB), and fulfil form factor requirements. The data acquisition is performed via a 1 Gbit Ethernet link and, for test purposes, a low rate optional readout via VME64 compliant interface is foreseen.
Since for each event a large fraction of channels will only contain pedestal counts, various zero suppression algorithms are foreseen to reduce the data flow to the experiment event building farm.
In addition to the data processing and readout, digitised signals from the selected channels are summed up to build a Trigger SUM (Super-Cell) and sent to the experiment trigger system. The selection of the channels contributing to a particular Super-Cell, as well as the number of Super-Cells formed in a module is programmable.
The Trigger SUMs are readout via 4 differential 640 Mbit/s serial links sharing one standard Ethernet cable.
All control, processing and communication functionalities of the board are implemented in a reconfigurable FPGA devices. The 'basic'firmware should not use more than 40% of device capacity, thus, new data processing and/or trigger algorithms can be developed, evolve and be integrated smoothly during the lifetime of the experiment.
In total, about 450 CREAM modules should be produced, tested and installed, in order to have the entire LKr calorimeter readout system operational by mid-2013.

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Session Classification: Posters

Track Classification: Systems