

Trigger-Less Readout Electronics for the PANDA Electromagnetic Calorimeter

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PANDA, the detector for antiProton ANnihilation at DArmstadt at the Facility for Antiproton and Ion Research (FAIR) in Germany

PANDA spectrometer employs fixed target and cooled antiproton beam:

- momentum range 1.5 GeV/c to 15 GeV/c
- Luminosity: $10^{31} - 2 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$

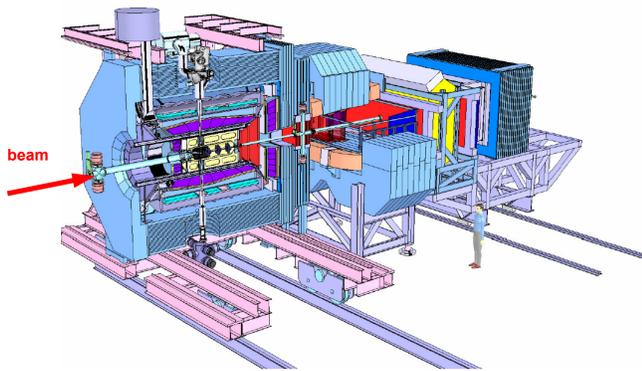
PANDA physics goal:

Shed light on

- origin of confinement
- origin of mass & spin
- degrees of freedom
- validity of QCD at long distance scale

by investigating

- hadron spectrum up to charm-quark mesons
- structure of nucleons



To achieve the physics goals, the PANDA event selection has to be:

- **Efficient:**
 - Detect physics signatures (e.g. secondary vertex, lepton pair with given invariant mass)
 - Handle *simultaneously* several different high-level event-selection criteria (efficient use of beam time)
- **Flexible:**
 - Lets each sub-detector contribute to the high-level selection
 - Can be reconfigured without modification of hardware
 - Is designed modular: same readout for sub-detector tests and for production experiments
- **Able to operate at very high rates:**
 - 20 MHz interaction rate → hit rate ~500 kHz

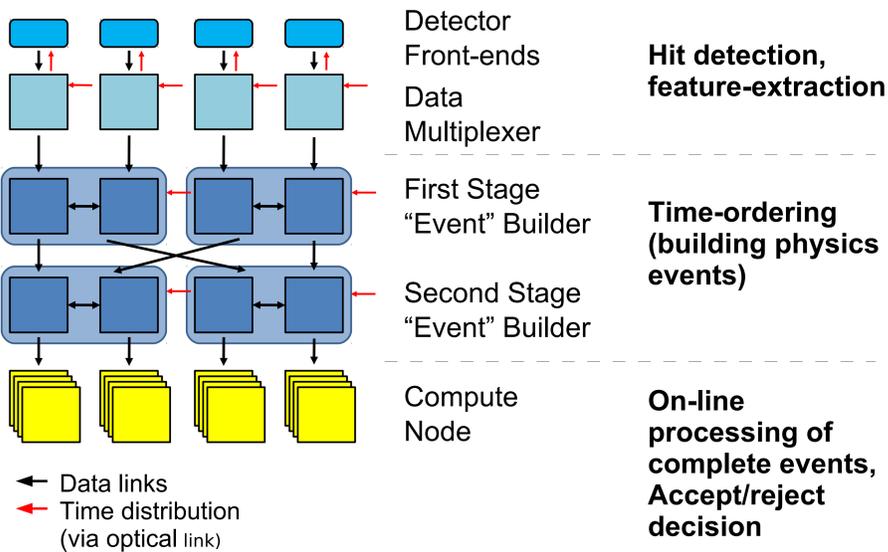
All requirements can be fulfilled

by constructing a **Trigger-less Readout:**

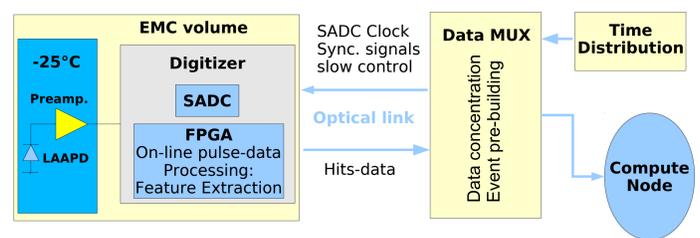
- **With self-triggered intelligent front-end:** autonomous hit detection and data preprocessing (e.g. based on **Sampling ADC**)
- **A very precise time distribution system:** single clock-source for PANDA
- **With time-sorted and processed on-line data:** processing in FPGA

Trigger-less Readout Concept

Bird's-eye view of the readout scheme



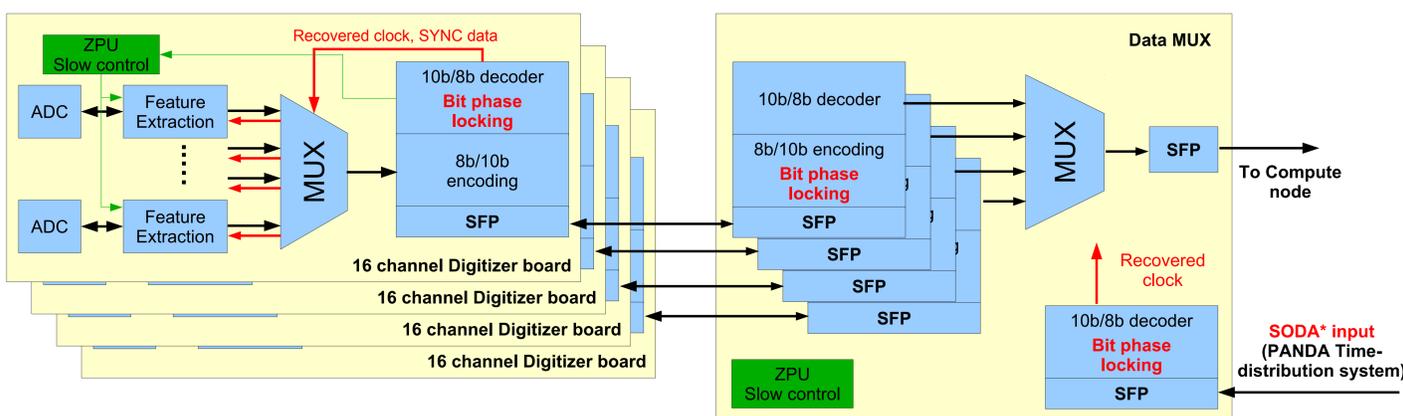
Readout for the PANDA Electromagnetic Calorimeter (EMC)



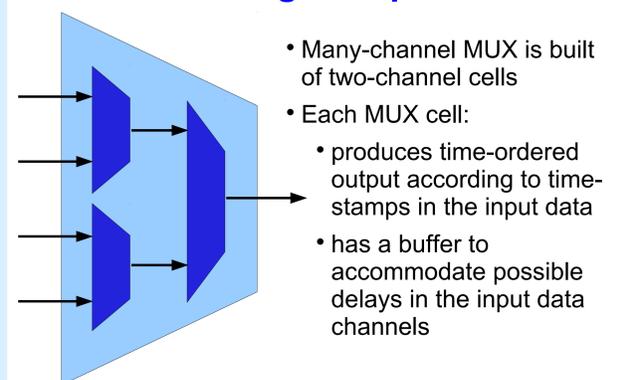
Key components of the readout:

- Digitizer module with **on-line pulse-processing**
- Data-multiplexer with **time-ordered output**
- **Synchronous optical-link connection** (clock-signal distribution)
 - **Standard** implementation **does not guarantee stable phase** of the recovered clock (phase changes at power/reset cycle) → special arrangement needed → **Bit phase locking**

Constructed Prototype of Readout-chain for EMC



Time-Ordering Multiplexer Unit



Bit Phase Locking with Xilinx FPGA (Serializer/Deserializer (SerDes) of Spartan-6, Virtex-5)

The Problem: the parallel clock, recovered by SerDes, may adopt 10 stable phase positions relative to the input serial clock → not useful for synchronization

Solution: The SerDes of the Xilinx FPGA can be configured such that a stable phase is guaranteed, however, the SerDes will lock on a signal only once in 10 trials (on average) → special state machine resets the SerDes until it is locked on a signal

Performed functional tests of:

- single SADC unit with complete functionality
- synchronous optical link (stability of the recovered clock-phase)
- time-ordering multiplexer unit

Used hardware components:



Summary and Outlook

- Trigger-less readout allows to bring detector performance to the highest level
- The first prototype of the PANDA trigger-less readout is ready for functional tests
- Future steps:
 - Test multi-SADC readout system
 - Couple developed readout hardware (SADC+MUX) with existing high-level on-line processing firmware for EMC (e.g. cluster finding)

* "SODA: Time distribution system for the PANDA experiment" : I. Konorov et al., NSS/MIC Conference Record, 2009 IEEE, DOI 10.1109/NSSMIC.2009.5402172.