

Trigger-less readout electronics for the PANDA Electromagnetic Calorimeter

Thursday 29 September 2011 16:00 (2h 30m)

The PANDA collaboration at the future FAIR facility at Darmstadt, Germany, will employ antiproton annihilations to investigate yet undiscovered charm-mesons and glueballs. The rich physics program requires various sophisticated event-selection criteria based e.g. on invariant mass, secondary vertices, and time correlations. Therefore, the readout electronics is designed such that all detectors may contribute to the event-selection process. The front-end electronics has built-in intelligence to extract and transmit only physically relevant information. A prototype of the corresponding readout chain was built for the PANDA Electromagnetic Calorimeter, based on sampling ADC readout and FPGA data filtering. The achieved results will be presented.

Summary 500 words

The aim of the investigation presented here is to develop the trigger-less readout of the PANDA Electromagnetic Calorimeter (EMC) and to construct a complete readout-chain prototype with all required electronic components. The PANDA EMC will be built of PbWO₄ scintillating crystals and will be employed for the detection of high energy photons, electrons and neutral mesons. The EMC will operate at high counting rates, up to 750 kHz per crystal. Therefore, the response of each detector unit must be kept as short as possible in order to reduce the amount of pile-up hits. For the remaining pile-up hits a recovery procedure is foreseen. The PWO crystals will be read out by large-area avalanche photo diodes (LAAPD) and vacuum photo triodes (VPT) coupled to low-power and low-noise preamplifiers. In order to implement the trigger-less readout concept for the EMC the preamplifier signals will be continuously digitized by sampling ADCs (SADC) and the data will be processed on-line in FPGAs by a feature-extraction algorithm. Such processing allows to fulfil all above mentioned requirements, e.g. pile-up recovery.

The designed readout includes a dedicated SADC, data multiplexer (MUX) and data-acquisition (DAQ) modules, where several SADC digitizers will be connected to a MUX module by optical link. From the MUX data will be streamed to the data acquisition. The trigger-less readout concept requires precise time-synchronisation of all data acquired by the digitizer modules. Therefore, all SADCs should use the same clock source and there should be a possibility to simultaneously set the zero-time for all digitizers. Due to mechanical and electrical constraints only serial optical-link connections are possible between the EMC digitizers and the rest of the DAQ. Therefore, as a key requirement, the clock and time information should be distributed using these optical connections. The standard implementation of the serial optical data-links does not guarantee a stable phase of the recovered clock signal on the receiver side with respect to the transmitter side, namely in case of power-up cycles. This problem can be omitted by using a specially designed communication protocol and a modification of the hardware, related to the optical-link transceivers/receivers. In this work we found that for the Xilinx FPGA a synchronous serial optical-link connection can be established by applying special settings to the FPGA serializers or deserializers and building a specialised state-machine which is establishing and monitoring a connection. This approach was tested using a set-up built of two different test boards with Xilinx Virtex-5 and Spartan-6 FPGAs. Test measurements demonstrated that the recovered clock was always in phase with the master clock disregarding the power cycles of the receiver board, while with the standard setting of the serial link, the phase took randomly one of ten possible values after each power cycle.

The presented EMC readout-chain prototype will include a dedicated SADC module with specially designed firmware with hit detection and processing algorithm, a FPGA-based data-acquisition module and the time-distribution system. The presentation will discuss the design goals, the implementation and first test results achieved with the readout chain.

Primary authors: Mr SCHREUDER, Frans (KVI, University of Groningen); Mr TAMBAVE, Ganesh (KVI, University of Groningen); Prof. LÖHNER, Herbert (KVI, University of Groningen); Mr HEVINGA, Michel (KVI, University of Groningen); KAVATSYUK, Myroslav (KVI, University of Groningen); Mr LEMMENS, Peter (KVI, Uni-

versity of Groningen); Mr SCHAKEL, Peter (KVI, University of Groningen); Mr SPEELMAN, Rene (KVI, University of Groningen)

Presenter: Mr LEMMENS, Peter (KVI, University of Groningen)

Session Classification: Posters

Track Classification: Systems