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Level-1 track triggers for the ATLAS high luminosity upgrade

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The HL-LHC, the planned high luminosity upgrade for the LHC, will increase the collision rate in the ATLAS detector approximately a factor of 5 beyond the luminosity for which the detectors were designed, while also increasing the number of pile-up collisions in each event by a similar factor. This means that the level-1 trigger must achieve a higher rejection factor in a more difficult environment. This talk will discuss the challenges that arise in this environment and strategies being considered by ATLAS to include information from the tracking systems in the level-1 decision. The main challenges involve reducing the data volume exported from the tracking system for which two options are under consideration: a region of interest based system and a intelligent sensor method which filters on hits likely to come from higher transverse momentum tracks.

Summary 500 words

The ATLAS upgrade for the HL-LHC will include a complete replacement of the inner detector (tracking system). The current design is to have an all silicon tracker with a combination of pixel and silicon strip detectors. In order to have a broad physics potential it is desirable to include information from the tracking systems early in the trigger decision. One possible solution is to use a region of interest driven readout for triggering. The level-1 trigger would be split into two steps: level-0 and level-1. Data from the front end electronics would propagate through a pipeline for up to ten microseconds as it does presently. A fixed delay, beam synchronous, level-0 trigger based on information from the calorimeter and muon systems would identify data of interest to be stored in an on chip buffer. In the level-0 time frame or slightly longer a Regional Readout Request (R3) would be sent to a small portion of the inner detector tracker where calorimeter and muon data predict that a candidate particle has passed. The data from these regions would be readout and used in a fast tracking algorithm for an asynchronous level-1 decision. The design criteria, feasibility, and initial work on the implementation will be presented. The primary focus will be on the latency and data flow design for communication between the external processing and the detector front ends.

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