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# GOSSIPO-4: an array of high resolution TDCs with a PLL control

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GOSSIPO-4 is a prototype chip featuring an array of high resolution Time to Digital Converters (TDC) with a PLL control that will be taped out on the 9th of August 2011. This prototype is the successor of GOSSIPO-3 test chip and the precursor of the 65k pixel TimePix3 chip. The prototype is being developed to test a set of new features that will be used in TimePix3, including a 8 pixel structure sharing one fast oscillator with a new topology, a PLL to provide the control voltage to the oscillators, a custom fast counter and a new small-area cell library.

## Summary 500 words

Tests performed on the GOSSIPO-3 have shown the reliability of the analog frontend, the reproducibility of the characteristics of the pixel across different chips and the foreseen properties for the Low Drop Out Regulators. Nevertheless a big Differential Non Linearity of the TDC and crosstalk effects between the reference clock (40 MHz) and the fast clock used to perform high resolution time measurements (580 Mhz) have been observed. These effects are still not fully reproduceable in simulations. Given these premises a new design has been planned in the framework of the TimePix3 chip: to overcome these problems, GOSSIPO-4 uses a 8 pixel structure that shares a PLL voltage controlled oscillator in contrast with GOSSIPO-3 where each pixel had his own oscillator. In addition, the topology of the oscillator has been changed to be less sensitive to any non uniformity on the supply voltage, which is most likely the main source of the effects we see in GOSSIPO-3.
The demands from the gaseous detector community for a high resolution Time Projection Chamber (TPC) are challenging and the space available on the single pixel of TimePix3 is an important issue: the above mentioned 8 pixel structure with shared oscillator is one of the measures to minimize the circuit area. In addition, a new library of minimum area standard cells has been designed at CERN and will be extensively used in GOSSIPO-4: this library has never been used in a fabricated chip before and we aim to prove that the characteristics of the cells are in agreement with those we obtained from automated characterization.
While these minimum area cells can be used for normal speed operations (40 MHz), they are not suited for blocks in the TDC which run at 640 MHz clock frequency. Hence, two full custom blocks, the fast counter and the synchronization logic, have been designed. These two designs not only fit better our needs in high precision measurements but help avoiding metastability problems that can occur in the design.
An additional change in GOSSIPO-4 is the use of a regular 4-bit counter instead of a Linear Feedback Shift Register; although slightly larger than a LFSR, it eases the PLL design because it is possible to use a normal power-of-2 divider.
With the GOSSIPO-4 prototype we hope to prove that high resolution time measurements with the proposed structure are possible and tolerant to parasitic effect and can be successfully implemented in TimePix3.

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