A READOUT SYSTEM-ON-CHIP FOR A CUBIC KILOMETER SUBMARINE NEUTRINO TELESCOPE

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The KM3Net Detector

Digital Optical Module (DOM)

31 PMTs/DOM

12800 DOMs

320 lines

http://www.km3net.org

The DOM processor board

Power conversion board

Processor board & Software designed at CEA-IRFU

DOM designed at NIKHEF institute (Amsterdam, Netherlands)

HV PMT base

Heat conductor

PMT

Signal collection board
The KM3Net prototype
Offshore Processor Board

- PMTs
  - 31 TOT Data
  - x 31 small PMTs

- FPGA
  - Bitstream
  - Processor Boot
  - Flash Memory (32 MB)
  - Slow-Control
    - for the Storey (I2C, SPI)

- 31 x 1 GHz TDC

- Readout Logic

- Slow-Control Task
  - Readout System On Chip (RSOC) / VIRTEX-5 PPC440 processor

- Data
  - SC Protocol Logic
  - Clock / Command Extraction

- DDR2 Memory (64 MB)

- RTOS

- 1Gb/s Ethernet Link
  - To shore station

- Data Task
  - Slow Control Task
Firmware TDC Development

Packetized and Sent over ETHERNET

Event type/TDC number

Coarse Time Stamp #24-bit

TDC #16-bit

XILINX VIRTEX-5 ISERDES

[Originally designed by A.Zwart (NIKHEF) / small PMTs test bench for ALTERA]
Clock distribution

Command (CMD) insertion

Custom Logic

Phase and Latency Measurements

Transmit Reference Clock @62.5 MHz

STANDARD 1000BASE-X ETHERNET

On Shore VIRTEX-6 Board

Command (CMD) extraction

Custom Logic

Recovered Clock @62.5 MHz / Bit slice analysis (known latency)

Recovered Clock @62.5 MHz

IDLE CMD DATA

1.25 Gbps

1000BASE-X ETHERNET

1.25 Gbps

Event Time Stamping

PPC440 Bus

Embedded 62.5 MHz

DATA

CMD
Transmit/Receive clock skew

Tx/Rx clock skew measured on shore with DMTD and oscilloscope (ns)
Store & Forward Acquisition model

PMT 0-31 & Routing Matrix

31 TDC & Routing Matrix

Acoustic Data

Detector Clock (ETHERNET)

PPC440 processor @ 300 MHz 1 Gb/s Ethernet Port

31 TDC

Circular Buffer

FIFO 0

FIFO 5

Data Router

FIFO 6

PMT 0-31

Readout Logic

FIFO 0

FIFO 5

FIFO 6

Dynamic Memory

134 ms Data

Interrupt @ 134 ms (Typical)

Slow control (Configuration, Readout on requests)

134 ms Data

134 ms Data

Time Slice To Computer 1

Time Slice To Computer 2
Time Slice Building

**Intrinsic Parallelism**

**Embedded Computing**

- Time Slice 2
- Time Slice 1
- Time Slice 0

**Start**

**Detector Clock (Start) Commands**
- Track reconstruction
- Data routing

**Clock Distribution/Commands Insertion**

**Multi-gigabit Standard Ethernet Switching**

**Onshore Farm**

**Offshore Nodes**

**Farm Computing**

**Performance Parallelism**
**Data acquisition setup**

**Reference Clock** @62.5 MHz

**STANDARD 1000BASE-X ETHERNET**

**On Shore VIRTEX-6 Board**

- Run Control
- Target Configuration
- Data acquisition
- vxWorks RTOS boot server

**RSOC VIRTEX5FX-70**
- vxWorks RTOS
- 1 TDC Channel
- 1 dedicated TDC ASIC channel
- PPC440@300 MHz
- Bus@75 MHz

**Pulse generator**

**Synchronous 1000BASE-X ETHERNET**

**Start Command**

**Reference Clock** @62.5 MHz

**Host PC**
Acquisition results

Scope measurement
Mean: 100,10667 µs
RMS: 1,75 ns

Power: 7 W

Pulse @ f=10 kHz
2 ns 8 ns 2 ns

Current acquisition setup (Source limitation): 60 Mb/s

Standalone measured TCP/IP throughput
PPC440@400 MHz / Bus@100 MHz / WindRiver Zero Copy buffer / Jumbo frames: 988 Mb/s
CONCLUSION

- Common Readout system functions integrated in a single component (RSOC):
  - Event Time stamping @ 1 GHz
  - Clock and command distribution
  - Slow-control and data acquisition performed in a RTOS multi-tasking embedded system

- RSOC is a node designed to be plugged in a complete Data acquisition System
  - Server/Client topology (ICE)
  - Scalable system