A 16 Channel High Resolution (<11 ps) Time-to-Digital Converter in a Field Programmable Gate Array

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Outline

- Introduction - Motivation
- Background
  - Architectural methods
  - Time interval averaging method
- Implementation of Tapped-Delay Line
  - Architecture of Time-to-Digital Converter
  - Architectural effects of FPGA
  - Wave union launcher
- Measurements
  - Static error & resolution
  - Resource consumption & important parameters
- Conclusion & Outlook
Introduction - Motivation

- Motivation
- Area of application; HADES, PANDA, Daisy, CERN etc.
- Purpose of the project
Introduction - Motivation

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Architectural Methods

- Coarse measurement method
- Fine measurement methods
  - Time stretching
  - Double conversion
  - Vernier method
  - Tapped delay line method
- Interpolation methods
Tapped Delay Line Method

- Composed of a number of delay elements with propagation delay of \( \tau \)
- Measurement result:
  \[ T = n \cdot \tau \]
- Thermometer code to binary code converter is needed
- Fast conversion time
- Number of delay elements:
  \[ N = \frac{MR}{\tau} \]

MR: Measurement range
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Architecture of Time-to-Digital Converter

- LUTs used as delay elements
- Fast carry-chain structure
- Registers exist in the same slice

Lattice ECP2M FPGA Slice Diagram
Architecture of Time-to-Digital Converter

Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floorplan

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Architecture of Time-to-Digital Converter

Bubble Error!!!
Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture
Architectural Effects of FPGA

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Architectural Effects of FPGA

Bin width histogram of a channel with shorter routings

Mean: ~10 ps
Max: ~35 ps

Bin width histogram of a channel with longer routings

Mean: ~15 ps
Max: ~45 ps
Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture
Wave Union Launcher

- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher [8] is implemented
- Bin widths & non-linearities are reduced
Wave Union Launcher

- More virtual bins
- Narrower bins
- Homogeneous bin distribution

Bins: ~240
Mean: ~20 ps
Max: ~45 ps

Bins: ~520
Mean: ~10 ps
Max: ~35 ps
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Measurement Setup

EXPLODERv1
Statistical Error & Resolution

- Time difference measured between 2 channels
  \[ \Delta t = (t_{\text{coarse1}} - t_{\text{coarse2}}) - (t_{\text{fine1}} - t_{\text{fine2}}) \]
- RMS measured: 10.34 ps against same clock
- Resolution: \( 10.34 \text{ ps} / \sqrt{2} = 7.3 \text{ ps} \)
- Effect of 2 transitions:
  \( 14.82 \text{ ps} / 10.34 \text{ ps} = 1.43 \text{ factor} \)
Mean Time Measurements

Mean time measurements for different cable length differences
Stability

RMS change over time

Max change 0.15 ps

Mean change over time

Max change 2.5 ps

340.000.000 hits
Extra Feature – Trigger Window

- Fixed signal relative to the trigger.
- 1 MHz Random signal
- 500 ns post-trigger window
### Resource Usage & Important Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resource (slice)</td>
<td>57% of ~24K slice</td>
</tr>
<tr>
<td>Resource (LUT)</td>
<td>40% of ~50K LUTs</td>
</tr>
<tr>
<td># of channels</td>
<td>16</td>
</tr>
<tr>
<td>Max bin width</td>
<td>34 ps</td>
</tr>
<tr>
<td>Avg. bin width</td>
<td>~10 ps</td>
</tr>
<tr>
<td>RMS</td>
<td>10.3 – 12 ps</td>
</tr>
<tr>
<td>Max conversion time</td>
<td>45 ns</td>
</tr>
<tr>
<td>Dead time</td>
<td>30 ns</td>
</tr>
<tr>
<td>Carry chain length</td>
<td>320</td>
</tr>
</tbody>
</table>
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### Conclusion
- 16 channels implemented in 50K LUT Lattice FPGA
- \(~10\) ps RMS is reached with 2 transitions
- Avg. bin width \(~10\) ps, yielding long delay line
- Very good results with one of the cheapest FPGA.

### Outlook
- Higher system clock frequency, 400MHz
- Remove double synchroniser
- Reduce resource consumption
- Implement more channels, 64
- Reduce dead time
TRBv3

- 256 channel on board
- ~10 ps RMS
- FEE, Readout on-board
- Will be used for Hades, PANDA, CBM, etc.
- Per channel cost similar with ASIC-HPTDC from CERN, but 10 times higher resolution!!!
References

[1] G. Otto, Presse und Kommunikation, GSI Helmholtzzentrum für Schwerionenforschung GmbH, G.Otto@gsi.de


