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A 32-Channel High Resolution (<15 ps RMS) Time-to-Digital Converter (TDC) in a Field Programmable Gate Array (FPGA)

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A 32-channel Time-to-Digital Converter (TDC) was implemented in a general purpose Field-Programmable Gate Array (FPGA). The fine-time calculations are achieved by using the dedicated carry-chain lines. A low latency (30 ns) encoder handles the conversion of the fine time measurement. The coarse counter defines the coarse time stamp. In order to overcome the negative effects of temperature and power supply dependency bin-by-bin calibration is applied. The time interval measurements are done using 2 channels. RMS and the time resolution of channels are calculated for different time intervals and a minimum of 15 ps RMS on two channels, yielding 10.6 ps (15ps/$\sqrt{2}$) time resolution on a single channel is achieved.

Summary 500 words

A 32-channel Time-to-Digital Converter (TDC) was implemented on a Lattice ECP2M Field-Programmable Gate Array (FPGA) for physical experiment measurements, such as Time-of-Flight (ToF).

Each channel has an individual fine counter, an encoder and a First-In-First-Out memory block (FIFO). A common coarse counter, operating at 200MHz, generates time stamps for the time information of each conversion. The time-to-digital conversion and the data read-out are undertaken at 200 MHz and 100 MHz clock frequency respectively and both time references were generated by an on-chip Phase Locked Loop (PLL).

The time interval between the rising edge of a hit signal and the rising edge of the next system clock is measured at the fine counter. The fine time interval calculations are achieved with a Tapped-Delay-Line (TDL) method, using the dedicated carry-chain lines of the FPGA. A multi-bit adder structure is used in order to form the delay line. The result generated by the fine counter in thermometer code [1] is converted to a binary code in the low latency (30 ns) encoder and stored in the FIFO with a time stamp generated by the common coarse counter as well as a channel number. In order to overcome the negative effects of temperature and power supply dependency the data is calibrated off-line, using the bin-by-bin calibration method [2].

In our measurements we used two channels in order to measure the time difference between two hits signals. A Tektronix Data Timing Generator DTG5078 generated the hit signals. Sets of measurements with different time differences were done in order to test the stability and the consistency of the TDC. For each measurement data of 300 000 hits were collected and analysed.

The time difference was increased logarithmically starting from zero up to one microsecond in order to observe the effects on the measured mean value and RMS. The RMS calculated for the time differences for up to two clock periods (10 ns) was 15 ps. As two channels were used in order to determine the time measurements, the time resolution of a single channel was 10.6 ps (15ps/$\sqrt{2}$).

With the rising time differences, the resolution of the TDC decreased and reached 35 ps for 1 us time difference. This deviation is caused by the jitter induced from the PLL used as the time reference.

In order to observe the temperature dependency of the TDC, a series of measurements between 48°C and 80°C were done. As the temperature increases, the propagation time along the delay line decreases. Therefore, malformations were observed in the calibration look-up-table. In parallel, the RMS value declined. However, updating the calibration look-up-table for the current temperature value overcame this problem.

Some of the important parameters of the designed TDC are as follows: Maximum bin width 48 ps, average bin width 20 ps, highest time resolution 15 ps, maximum conversion time 45 ns, dead time 30 ns, delay chain length 288.

A 32-channel high resolution TDC based on the TDL method is implemented in a Lattice-ECP2M FPGA and a time resolution of 15 ps was achieved at each channel.

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