Studies for the detector control system of a future ATLAS-pixel detector

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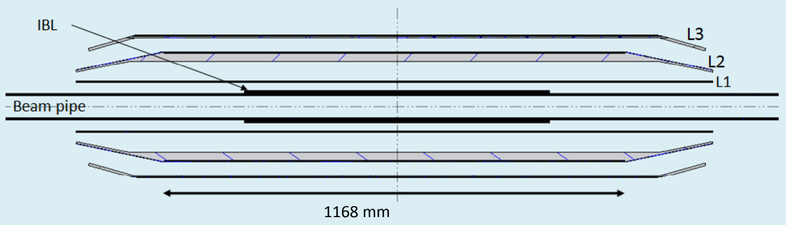
In the context of the LHC upgrade to the HL-LHC the inner detector of the ATLAS experiment will be replaced completely. As part of this redesign there will also be a new pixel detector. This new pixel detector requires a control system which meets the strict space requirements for services and electronics in the ATLAS experiment.
To accomplish this goal we propose a DCS (Detector Control System) network with the smallest form factor currently available. This network consists of a DCS chip located in close proximity to the interaction point and a DCS controller located in the outer regions of the ATLAS detector. These two types of chips form a star shaped network with several DCS chips being controlled by one DCS controller. Both chips are manufactured in deep sub-micron technology.
We present prototype tests with emphasis on studies concerning radiation effects, especially single event upsets (SEU).

The new ATLAS Pixel Detector

For the new ATLAS inner detector a pixel detector is under development. Following design criteria are:

- Detector modules are mounted on staves
- At both ends of each stave there is an End-of-Stave card (EoS-Card)
- Detector layout:
  - Staves oriented in parallel to the beams are mounted on cooling pipes next to each other to form barrels with different diameters (layers)
  - Coaxial layers with different diameters around the beampipe form the barrel section of the pixel detector
- Pixel ≤ (50 x 250) µm²
- |η| ≤ 2.5
- Radiation dose
  - 570 Mrad
  - $2.4 \cdot 10^9 \frac{particles}{cm^2 \cdot s}$

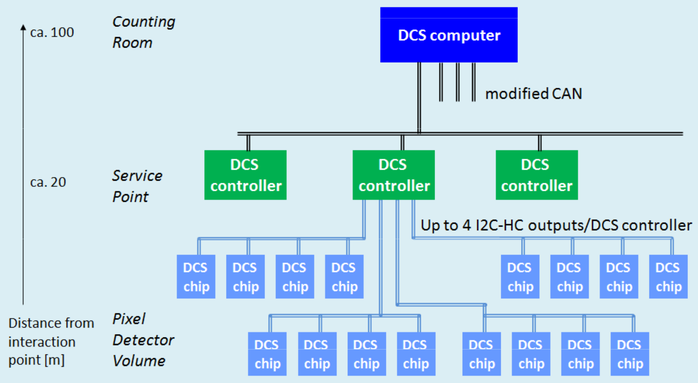


Possible layout partly taken from E. Anderssen et al. AUW Nov 2010

DCS Network

The DCS network is the control & feedback path. It is a compromise between highest possible reduction of cables and minimization of risk to lose control of DCS items.

- Consists of DCS chip and DCS controller
- DCS chip located at the EoS-Card
- DCS controller located at a service point (20 m from the interaction point)
- 4 x 4 DCS chips are connected to one DCS controller
- DCS controller is connected to the DCS computer in the counting room
- Connection between DCS chip and DCS controller via differential lines due to the length of cables with a baud rate of 100 kbaud
  - Signal transmission inspired by CAN bus
- Data transfer between DCS chip and DCS controller via I2C-HC
  - I2C-HC is a modified I²C protocol which was extended by a (12,8) Hamming code to allow correction of single bit flips and detection of dual bit flips



DCS Requirements

To ensure a stable and reliable operation of the ATLAS Pixel Detector the detector control system has to meet several requirements:

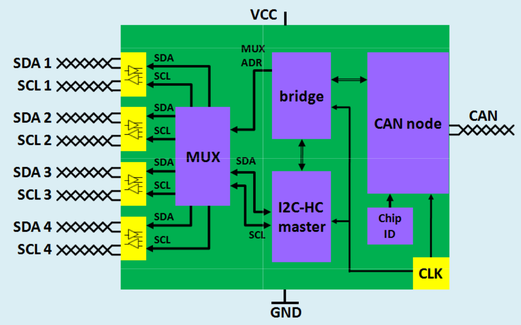
- Low material cost and impact onto the measurements of the other ATLAS subdetectors
- Radiation hard
- Low power consumption (passive cooling)
- Easy to integrate into the ATLAS DCS framework
- Reliable monitoring and steering of all operation relevant quantities:

Component	Monitored values		Controlled values
Modules	HV	Current & Voltage	Voltage setting & On/Off
	LV	Current & Voltage	Voltage setting & On/Off
		Temperature	
End of Stave Cards	Current & Voltage		Voltage setting & On/Off
	Temperature		
			Reset
On detector Opto transceiver	Current & Voltage		Voltage setting & On/Off
	Temperature		
			Reset
Environment & Cooling	Humidity		
	Temperature		

Each of these values has individually defined properties in

- Severity
- Availability
- Granularity
- Location of processing

DCS Controller



Requirements:

- Radiation hard
- As few lines as possible
- CAN node
- Master of the DCS chip interface
- Bridge between interface abd node
- Multiplexer connects I2C-HC master to the corresponding bus

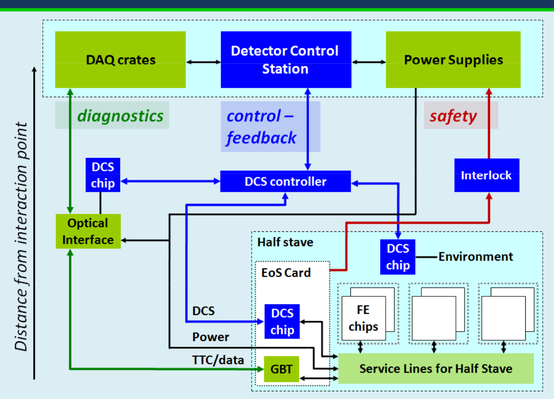
Connection to outer world:

- Power, data and clock will have own lines
- DCS chip data is communicated to the counting room via CAN

First prototype contains:

- CAN node
- I2C-HC master
- Bridge

DCS Architecture



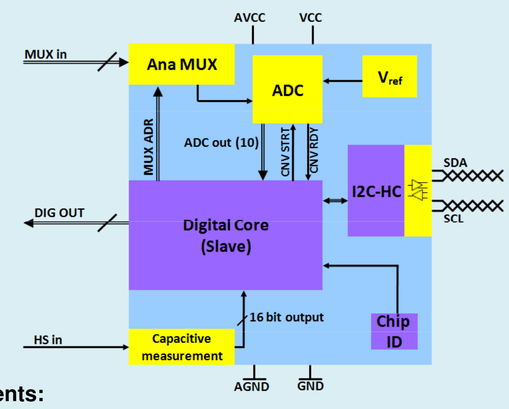
DCS oversees detector modules, EoS-Card, optical interface and monitors the environment. Its splitted in three paths:

- **Safety**
  - Always on
  - Highest reliability
  - Low granularity
  - Hardwired interlock system
- **Diagnostics**
  - On request during calibration
  - Per front end chip
  - Data is merged into data path
- **Control & Feedback**
  - For all use cases
  - High reliability, independent of data path
  - Steering and monitoring of modules, end of stave card, optical interface
  - Per detector module or half stave

Steering is hierarchially divided into three groups:

- Per Half Stave
- Per Module
- Per Front End

DCS Chip



Requirements:

- Radiation hard at innermost layer of the pixel detector
- As few lines as possible
- Communication interface
- Low power consumption (for operation without cooling)
- Suitable for serial and parallel powering concept
- 16 ADC channels
- 2 16-bit counters + 2 identical working RC oscillators for capacitive humidity measurements
- 8 digital outputs

Connection to outer world:

- Power, data and clock will have own lines
- Data is sent via a differentially wired I2C-HC bus to master located at service point

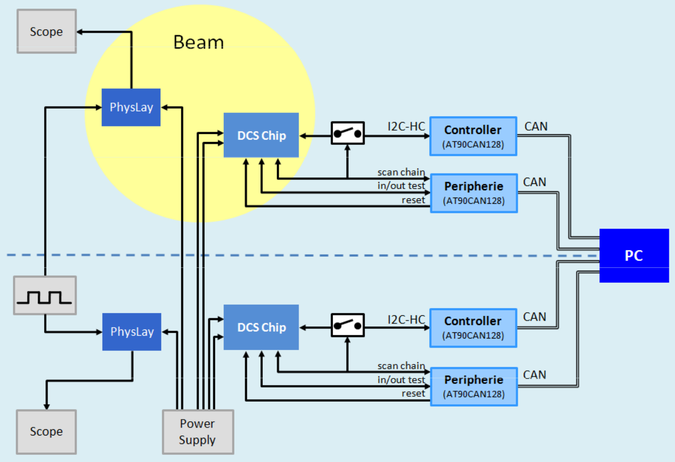
First prototype contains:

- I2C-HC slave
- ChipID

Irradiation test setup

In an irradiation test two prototype chips with different components of the DCS network were irradiated at the Paul Scherrer Institute in Villigen with the following parameters:

- 100 MeV proton beam energy
- Fluxes up to $5 \cdot 10^8 \frac{p}{cm^2 \cdot s}$
- $6.4 \cdot 10^5$ rad total dose

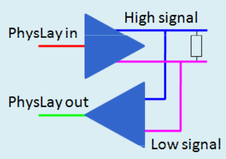


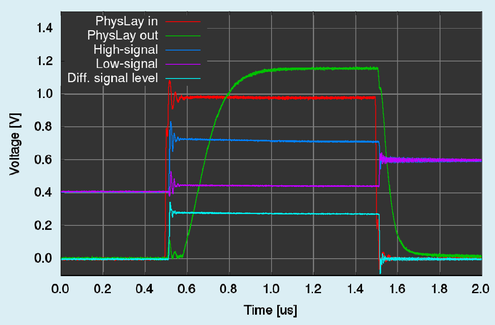
All chips were operated during the irradiation to test for radiation induced errors in functionality.

Irradiation: Physical Layer

The PhysLay1 chip is a prototype for the physical layer blocks of the DCS chip and the DCS controller. The chip contains two transceivers for antiparallel data transmission with a maximum voltage of 300 mV between the transmission lines.
During irradiation a reference chip and a chip in the beam were tested for stability in the following aspects:

- Transition times
- Signal delay



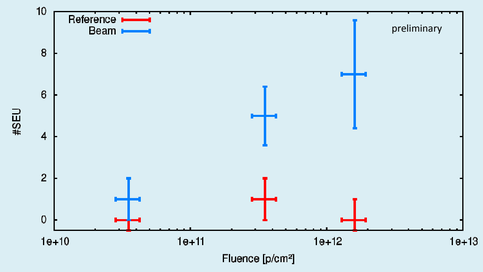


Once every minute the oscilloscope screen was saved.
There was no change of the signal's shapes within the errors during the irradiation. The chip's functionality was entirely maintained.

Irradiation: DCS chip

During the irradiation the DCS chip was operated in two different modes:

- Communication:
  DCS communication of normal detector operation was simulated during the irradiation
- Scan chain:
  In this mode, all registers of the chip are connected to one shift register which is read out and resetted frequently to observe SEUs



- 5 h of DCS communication were entirely faultless
  - No read/write errors in transmissions
  - TMR cleaned out all errors
  - The I2C-HC error correction had not to be fallen back on
- SEU crossection was preliminary determined to be in the range between $\left(1 \cdot 10^{-14} - 6.6 \cdot 10^{-14}\right) \frac{cm^2}{bit}$