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Studies for the detector control system of the new ATLAS Pixel detector

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In the context of the LHC upgrade to the HL-LHC the inner detector of the ATLAS experiment will be replaced completely. As part of this redesign there will also be an new pixel detector. This new pixel detector requires a control system which meets the strict space requirements for electronics in the ATLAS experiment. To accomplish this goal we propose a DCS (Detector Control System) network with the smallest form factor currently available. This network consists of a DCS chip located in close proximity to the interaction point and a DCS controller located in the outer regions of the ATLAS detector. These two types of chips form a star shaped network with several DCS chips being controlled by one DCS controller. Both chips are manufactured in deep sub-micron technology. We present prototypes with emphasis on studies concerning single event upsets.

Summary 500 words

In the context of the LHC upgrade to the HL-LHC the inner detector of the ATLAS experiment will be replaced completely. As part of this redesign there will also be a new pixel detector. This new pixel detector requires a control system which meets the strict requirements for electronics in the ATLAS experiment as the most important are: most possible reduction of dead material and radiation hardness for doses up to 570 MRad for ten years of operation. The protection against single event upsets (SEU) is crucial to ensure save operation as one of the control system's task is to switch on/off several parts of the detector. To meet these requirements, a completely new detector control system (DCS) is developed from scratch. This DCS consists of three independent paths: a safety path (hard wired interlock system), a control and feedback path (controlling the detector) and a diagnostics path (high granularity read out during calibration). We are concentrating on the control and feedback path which we realized in form of a star shaped network. This network consists of two types of nodes which are, to meet the space requirements, realized in the smallest available form-factor, an ASIC. The first node is called DCS-Chip and is located at the end of each half stave on the EOS-card. This DCS-Chip contains analog circuitry to measure environmental and detector conditions and digital circuitry to switch power of each module of its corresponding half stave. The acquired data is collected by the DCS-Controller node which reads out 16 DCS-Chips each and transmits this data to the counting room. The DCS-Controller contains only digital circuitry and is located at the outer patch panels of the ATLAS detector. To ensure safe communication over large distances between the two nodes, the data is transmitted differentially by a custom modified bus.

One of the latest outcomes of our research is the CoFee1 chip assembly. These chips contain for the first time prototypes for both nodes in 130nm technology. As early prototypes these chips only contain digital circuitry to - amongst others - study the behavior of digital logic on ASIC level in high radiation with emphasis on SEU. The analog circuitry required for the generation of differential signals were tested in a second chip called PhysLay1. This chip contains a transmitter and a receiver for the bus mentioned above to make up a prototype DCS network. Both chips were tested before, during and after irradiation and the outcome of these studies are presented.

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