Radiation Tolerant Low Power 12-bit ADC in 130 nm CMOS Technology

Filipe Sousa
Paulo Moreira
José Machado da Silva
Outline

• Overview
  – Characteristics

• Architecture
  – Dual slope ADC
  – Bandgap calibration
  – Currents automatic calibration
  – WhisBone bus
  – Prototype

• Testing\preliminary results
  – Bandgap precision
  – Offset and Gain
  – INL
  – Crosstalk
  – Power consumption

• Summary
The Analog to digital converter is intended to be part of the GigaBit Transceiver – Slow Control Adapter [GBT-SCA] ASIC suitable for the control and monitoring applications of the embedded front-end electronics.

It will monitor different voltages and temperatures from outside chips in the electronics.

The communication to the chip will be made through a parallel bus.
## Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Reference clock frequency</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-30°C to +80°C</td>
</tr>
<tr>
<td>Input range</td>
<td>GND to 1 V</td>
</tr>
<tr>
<td>LSB (least significant bit)</td>
<td>244 µV</td>
</tr>
<tr>
<td>36 Input channels:</td>
<td></td>
</tr>
<tr>
<td>32 analog inputs</td>
<td></td>
</tr>
<tr>
<td>1 temperature sensor</td>
<td></td>
</tr>
<tr>
<td>3 internal voltage signals</td>
<td></td>
</tr>
<tr>
<td></td>
<td>[0 V; 0.6 V(bandgap); VDD/2]</td>
</tr>
<tr>
<td>Conversion rate</td>
<td>4 KHz = 250us [worstcase]</td>
</tr>
<tr>
<td>Power consumption</td>
<td>975 µW [normal operation] 843 µW [power save!!?]</td>
</tr>
<tr>
<td>Adjustable Bandgap</td>
<td>Fuses</td>
</tr>
</tbody>
</table>
The input signal is integrated during a fixed period.

A constant current is applied to discharge the capacitor.

The duration of the second phase is proportional to the input signal.

The comparator offset is cancelled by the dual ramp.
Dual-Slope ADC Basic Operation

$V_{in} \rightarrow G_m \rightarrow I_d \rightarrow V_C$  

- Charge cycle: $\Delta V_C^{\text{charge}} = \frac{V_{in} \cdot G_m \cdot 2^N \cdot T}{C}$
- Discharge cycle: $-\Delta V_C^{\text{discharge}} = \frac{I_d \cdot N_c \cdot T}{C}$
- Measurement: $\Delta V_C^{\text{charge}} = -\Delta V_C^{\text{discharge}} \Rightarrow V_{in} = \frac{N_d \cdot I_d}{2^N \cdot G_m}$
- Calibration: $\frac{I_d}{G_m}$

To optimise the use of the dynamic range of the capacitor voltage, $I_d$ and $G_m$ are calibrated independently.

Gm is optimized to maximize the dynamic range while maintaining good linearity.

Id is used to calibrate the conversion.
Architecture

```

Analogue Multiplexer

Transconductance circuit

Gm and Id calibration bits

Discharge circuit

Charge/discharge

Comparator

Conversion and Calibration Logic

Register bank

Wishbone interface

Bandgap

Bias

V_BG

Vdd/2

temp

V_BG

V_C (max)

preCharge

resetCap

V_BL

forceVmax

Vdd

V_C (max)

count[12:0]

Clk

Input Channel selection

Gm  and Id calibration bits

Charge/discharge

Analytics

Multiplexer

Analogue

BG

GM

V

BL

BL

(max)

(max)

V

V

dd

V

...
Transconductor and Current Sink: Basic principle

Programmable Transconductor

Programmable Current-Sink

$V_{in}$

$V_{bandgap}$

$gmCal[9:0]$

$I_{charge}$

$I_{discharge}$

$V_{bandgap}$

$idCal[9:0]$
Bandgap Calibration

- The bandgap voltage drifts slightly with the temperature, and due to process mismatches it is different from chip to chip.

- To set the bandgap voltage to a precise value within a temperature range a variable resistor was implemented.

- With an adjustable reference voltage it is now possible to set the chip to work in specific temperature, thus allowing a more precise automatic calibration.

variable resistor
ADC automatic calibration

- **1\textsuperscript{st} Bandgap calibration**
  - The band voltage is used as the reference for the ADC calibration

- **2\textsuperscript{nd} Discharge slope calibration:**
  - Calibrate the discharge current ($I_d$) so that:
    $$V_{C,\text{MAX}} - V_{BL} = \frac{2^N \cdot T \cdot I_d}{C}$$
  - This can be achieved by setting the capacitor to $V_{C,\text{MAX}}$ and count until $V_C$ reaches $V_{BL}$. If:
    - count > $2^N-1$, current is low
    - count = $2^N-1$, current is right
    - count < $2^N-1$, current is high

- **3\textsuperscript{rd} ADC calibration:**
  $$N_C = \frac{V_{BG}}{lV} \cdot 2^N$$
  - Measure the bandgap voltage. If:
    - count > $2^N \cdot [V_{BG}/1\text{ V}]$, gm is high
    - count = $2^N \cdot [V_{BG}/1\text{ V}]$, gm is right
    - count < $2^N \cdot [V_{BG}/1\text{ V}]$, gm is low
Wishbone bus

- The ADC is controlled by accessing the internal registers of the ADC through a WISHBONE interface.

- The WISHBONE interface is a system-on-Chip (SOC) interconnection architecture, which defines a parallel communication protocol between portable IP cores.

- The interface comprises data input/output and address buses, as well as a clock signal, a synchronous reset signal, and signals that regulate the data flow.

- The implemented Wishbone Slave Interface allows the user to read and write on the registers, as well as to select one of the ADC input channels, start an ADC conversion operation, and read the ADC output.
• For the prototype chip production:
  
  In order to test the wishbone bus functionality, the parallel bus was kept as the external link instead of adopting a serial protocol like I2C.

  The lack of space for more pads has limited the input channels external accessible to 8.

  However a resistor divider was added to the chip in order to feed the other channels.
Testing and preliminary results

• The functional and parametric tests were performed at CERN in the IC tester.

• A custom PCB was fabricated to be the interface between the ADC and the tester.

For simplifying the measurements there is an external connector for the bandgap voltage.

Connectors for the power supplies are also available, in order to power the board from a different power source other than the tester.
Bandgap precision

- The bandgap voltage can be trimmed from 620 mV to 452 mV.
  - The step value is of 166 μV

- The bandgap voltage can be manually modified by acting in the bandgap registers.

- It can also be hardcoded by fusing the fuse bank as desired.

Bandgap programming

![Graph showing bandgap programming](image)
Some noisy results

- Whenever trying to convert a constant voltage the result varies 5 LSB [in both directions]

- Using an external oscilloscope a 50Hz noise was detected
  - With peaks of 4 mV

- When physically disconnected from the tester and powered with a battery the bandgap doesn’t contain that noise.
  - It is not possible with the present setup to feed the clock without connecting to the tester.

- However the mean value is the expected showing that the calibration is working
  - \(2457 = 0.6 \times 4096\)
Offset

- A systematic offset of 40 mV is observed.
- Since this architecture is immune to offsets from the comparator side,
  - one possibility is that there is a voltage drop before the comparator,
  - It can be also a charge sharing problem.
The ADC gain can be adjusted, with the manual calibration.

From a maximum of 5960 (normalized = 1.45) to a minimum of 3038 (0.74)

However the automatic calibration implemented sets the gain to around 4421 (1.08)
• The integral non linearity calculated from the ramp response.

• From 150 mV to 900 mV INL of 8 LSB
Crosstalk

- The voltage variations in adjacent channels affect the value measured.

Measuring:
- 700 mV channel input
- Adjacent channel sine wave 0 to 1V
- Variation measured ≈ 2.5 mV
Power Consumption

- Digital domain
  - 360 µW

- Analog domain
  - 612 µW [normal operation]
  - 480 µW [power save mode]

- Consumption in the power save mode comes from the Bandgap and the bias circuit.

- Power-off circuitry was not included on those to avoid interference during normal operation.

- Digital domain clock can be gated during the power save mode to reduce the digital domain power.
Conclusions

• The ADC was designed and is currently under tests.

• The state machine works as intended. And it is possible to write in all the configurations registers.

• However, in the analog side the preliminary results show some noise in the converter output. The source of the noise is yet to be identified, but probably it comes from the measurements instruments.

• The ADC presents a systematic offset; one of the possibilities is that is generated by some voltage drop before the transconductance circuit, or during switching [charge sharing].

• With the observed noise the ADC resolution is of 9 bits, which is equivalent to a LSB of 2,2 mV instead of the 244 uV.

• More tests will follow in order to validate the circuit.
Thank you ...
Detailed circuits

- The maximum charge current was set to 500 nA

- $V_C$ voltage range: 250 mV to 900 mV
  - 1 LSB $I_{12\text{bit}} = 159 \, \mu\text{V}$

- Duration of charging phase $2^{12}$ clock cycles = 102.4 $\mu$s

- The duration of one conversion cycle in the worst case is 250 $\mu$s which is equivalent to a frequency of 3.9 kHz

- Integrated capacitor:
  - $\Delta V = 650 \, \text{mV}$
  - $\Delta t = 102.4 \, \mu$s
  - $I = 500 \, \text{nA}$

  $$C = \frac{\Delta t \cdot I}{\Delta V}$$

- Capacitance: 78.76pF
  - A dual MIM capacitor is used to achieve linearity with reduced area.
    - 135 um X 135 um = 18225 um$^2$
Conversion and Calibration Logic

Conversion and Calibration Logic

- State Machine
- Counter
- Decoder
- Gated Clock
- Registers
- CLKN & CLKP
- HighP
- AdcCtrl
- Input signal select
- 72 = 36 x 2

Clocking:
- CLKN & CLKP

Signals:
- Counter control
- Counter out & overflow

Interfaces:
- To / From Wishbone Interface

Radiation Tolerant Low Power 12-bit ADC in 130 nm CMOS Technology
- **Reset**:  
  - Analog circuitry is turned off  
  - Data registers are cleaned.

- **Wake up**:  
  - Analog part is switched ON  
  - Time is given to let the circuit stabilize [70 us]

- **Ready**:  
  - The converter is ready for a conversion/calibration routine

- **Sleep**:  
  - Analog part is switched off. [Power saving mode]