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Radiation Tolerant Low Power 12-bit ADC in 130 nm CMOS Technology

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Electronic circuits submitted to high doses of radiation are prone to functional failures. Due to the high cost of currently available radiation hard technologies, alternative design approaches, resort to available, yet less costly and higher performance, commercial CMOS technologies. To improve radiation tolerance within these technologies specific design and layout methodologies are explored. In this work the design of a radiation tolerant low power 12-bit analogue to digital dual-ramp integrating converter (ADC) in 130 nm CMOS technology is presented. The rationale behind the selection of this architecture is described and details of the design of the ADC circuit elements are provided.

Summary 500 words

This paper addresses the design of a radiation hard 12-bit A/D converter to be used in the monitoring systems of High Energy Physics experiments (HEP) at CERN. The operation of the ADCs in the particle detectors exposes them to high radiation doses (> 100 MRad). In such environments, electronic circuits may see their performance degraded over time, are subject to charge transients, or even suffer catastrophic failures. Performance degradation is caused by the accumulation of trapped charges that are deposited by high energy particles impinging on the circuit. This type of degradation is commonly known as Total Ionizing Dose (TID) effects. Additionally, functional interrupts can be caused by single particles that upset temporarily the circuit operation. This type of events are denominated Single Event Upsets (SEU). To avoid TID effects specific semiconductor processes can be used to manufacture radiation hard ASICs. However, such processes are expensive and are not available in state-of-the-art CMOS technologies.

The purpose of the ADC presented in this work is to monitor detector environmental parameters such as, supply voltages, temperatures and other slow varying or DC signals. The input voltage range is 0 V to 1 V which the ADC should convert with a 12-bit resolution. This means that the targeted least significant bit width is 244 μV.

The analogue-to-digital converter designed uses a dual slope (DS) integrating architecture. This kind of architecture can achieve high accuracy (> 11 bits) for low conversion rates. It has a moderate circuit complexity when compared, with digital-ramp, and successive approximation converters, that use digital to analogue converters (DACs) in their design or even with the sigma-delta ones. Due to the slow varying or DC nature of the input signals being monitored a sample and hold circuit is strictly not needed in this application. The dual slope architecture requires an integrator and comparator and control logic. Compared with other architectures, a DS ADC has a potential for efficient use of, the silicon area and low power consumption. The intrinsic analogue integration involved in the dual-slope conversion operation reduces the effect of noise and transients in the input signal. This architecture provides therefore a good noise rejection. As a single baseline reference is used to start and finish the conversion the architecture is in principle insensible to the offsets in the comparator.

The ADC was designed as a macro cell to be integrated on an 130 nm CMOS ASICs for the HEP electronic systems. It includes an auto-calibration feature that allows to correct for effects of temperature, power supply voltage variations and, above all, for parameter changes induced by total ionizing dose over the life time of the device.
The ADC has a power saving mode which reduces up to 5 times the overall power consumption. Preliminary simulations show that nonlinearities smaller than ½ LSB can be obtained. Despite the fact that the converter is intended to be incorporated in another chip it was implemented as a standalone chip for test and validation purposes. The chip has been tapped-out for fabrication and experimental results will be included in the final version of the paper.

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