Contribution ID: **41** Type: **Poster**

# Timing Distribution for the Belle II Data Acquistion System

*Thursday, 29 September 2011 16:00 (2h 30m)*

At Belle II, most of the digitization is made inside or near the detector, and the digitized data are collected via high-speed optical serial links. Each of the frontend electronics boards equips at least one FPGA for a unified data link implementation, and at the same time to receive a system clock, the level-1 trigger and other fast timing signals and provide fast status signals. These timing signals are serialized and delivered via a commodity category-7 LAN cable, through a distribution network of cascaded 1-to-20 distribution modules. We report the initial performance test results of this timing distribution system.

## Summary 500 words

At the Belle II detector of the SuperKEKB electron-positron collider, most of the digitization is made inside or near the detector, and the digitized data are collected in a unified way via high-speed optical serial links, except for the innermost pixel detector system. Each of the frontend electronics boards equips at least one FPGA for the data link implementation, and at the same time to receive and provide a set of fast control signals. These signals include a 127 MHz system clock derived from the accelerator radio frequency clock, the level-1 trigger, initialization and synchronization signals, and other fast timing signals to provide fast status collection. These timing signals are serialized and delivered via a commodity category-7 shielded LAN cable, through a distribution network of cascaded 1-to-20 distribution modules. This module is in a double-width 6U VME form factor with 24 RJ-45 ports, or optionally with the same printed circuit board, with 16 RJ-45 ports and an FMC connector to attach a 8-port optical connection card. The optical connection is used to electrically isolate the network on the detector and another network in an electronics hut. The serial link for the timing signal is a 254 Mbps LVDS signal, and can be extended over 15 m LAN cable. The serialization and deserialization are directly performed by an inexpensive FPGA. Because no additional device is needed, 1+20 links fit in a 6U VME board. The clock signal and the timing signal are separately transmitted to guarantee a small jitter of the clock. At every step of the distribution, the clock signal is reshaped by a jitter cleaner, and the serial data is resynchronized. Three remaining RJ-45 ports are for a JTAG lines translated to the LVDS signals, for a 100-BaseT Ethernet connection, and for a multi-purpose LVDS ports. As we use JTAG lines on LVDS, we can distribute the LVDS signals with the same board to make parallel JTAG programming for the FPGAs in the frontend electronics boards. About 120 of this module will cover the timing and JTAG signal distribution over the entire Belle II data acquisition system. We report the initial performance test results of this timing distribution system.

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**Session Classification:** Posters

**Track Classification:** Systems